known. And to know the characteristics of the three configurations at a glance, we study their comparison in the tabular form given below :

S. No.	Characteristics	Common-base configuration	Common-emitter configuration	Common-collector configuration
1.	*Input resistance*	Low (50 Ω)	*Low (1 kΩ)	Very high (750 kΩ)
2.	*Output resistance*	Very high (500 kΩ)	High (10 kΩ)	Low (50 Ω)
3.	*Current gain*	Less than unity (0.98)	High (100)	High (100)
4.	*Voltage gain*	Small (150)	High (500)	Less than one
5.	*Leakage current*	Very small (5 μA for Ge 1 μA for Si)	Very large (500 μA for Ge 20 μA for Si)	Very large (500 μA for Ge 20 μA for Si)
6.	*Applications*	For high frequency applications	For audio frequency applications	For impedance matching

11.19. COMMONLY USED TRANSISTOR CONNECTION

Out of the three transistor configurations, the common emitter connections are used in about 90 to 95 percent of all the transistor application because of the following reasons :

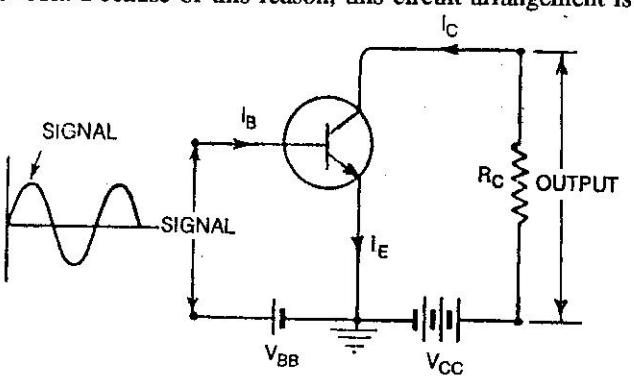
1. High current gain. In a common emitter connection, I_C is the output current and I_B is the input current. Since the value of output current I_C is much more than input current I_B, therefore, the current gain in CE configuration is very high. It may range from 20 to 500.

2. High voltage and power gain. As the output resistance is nearly 50 times to that of input resistance is CE circuit and because of high current gain, this type of transistor circuit arrangement has highest voltage and power gain. This is the major reason for using transistor in this circuit arrangement.

3. Moderate output to input impedance ratio. The ratio of output impedance to input impedance is quite small (about 50) in a common emitter circuit. Because of this reason, this circuit arrangement is ideal for coupling between various transistor amplifier stages.

11.20. TRANSISTOR AS AN AMPLIFIER (CE CONFIGURATION)

A common emitter *npn* transistor amplifier circuit is shown in Fig. 11.25. A battery V_{BB} is connected in the input circuit in addition to the signal. This battery provides forward *bias voltage* to the emitter-base junction of the transistor. The magnitude of bias voltage should be such that it keeps the emitter-base junction always forward **biased regardless of the polarity of the signal source.



npn transistor amplifier circuit

Fig. 11.25..

*We know that

$$\text{for } CB \text{ configuration, } r_i = \frac{\Delta V_{EB}}{\Delta I_E} \text{ at constant } V_{CB}$$

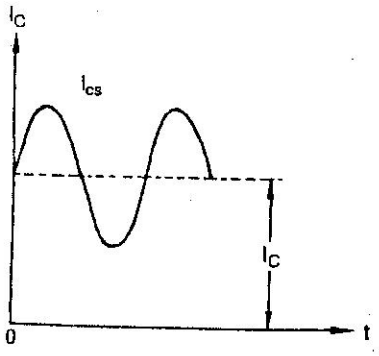
$$\text{for } CE \text{ configuration, } r_i = \frac{\Delta V_{BE}}{\Delta I_B} \text{ at constant } V_{CE}$$

From the above, it is evident that r_i for *CE* configuration is higher than *CB* configuration as the value of ΔI_B is in μA whereas, the value of ΔI_E is in mA.

**If d.c. bias voltage is not provided or its value is small, then during negative half cycle of the signal, the emitter-base junction will be reverse biased which will upset the transistor action.

Operation. When a *signal is applied in the emitter-base junction, during positive half cycle, the forward bias across this junction increases. This increases the flow of electrons from emitter to collector *via* base and thus increases the collector current. The increased collector current produces more voltage drop across the collector load resistor R_C. However, during negative half cycle of the signal, the forward bias voltage across emitter-base junction decreases. This decreases the collector current which consequently decreases the voltage drop across the collector load resistor R_C. Hence, an amplified signal appears across the collector load resistor.

Collector current analysis. The graphical representation of collector current is shown in Fig. 11.26. When no signal is applied, the input circuit *i.e.* emitter-base junction is forward biased by the battery V_{BB}. Therefore, a d.c. collector current I_C flows in the collector circuit. This current is called *zero signal collector current.* When the signal voltage is applied, during positive half cycle, the forward bias on emitter-base junction increases, causing increase in total collector current i_C. Whereas, during negative half cycle, the forward bias on emitter-base junction decreases which causes decrease in total collector current i_C. Thus, total collector current consists of two components, namely :



Graph for collector current

Fig. 11.26.

(*i*) The d.c. collector current I_C when no signal is applied. This is due to forward bias created at the emitter-base junction by the bias battery V_{BB}.

(*ii*) The a.c. collector current i_{cs} due to signal applied in the emitter-base junction.

$\therefore$ Total collector-current, $i_C = i_{cs} + I_C$.

The useful output is the voltage drop across collector load resistor R_C due to the a.c. component of current i_{cs} which flows through it because of applied signal. The purpose of zero signal collector current *i.e.* d.c. component I_C is only to ensure that emitter-base junction is forward biased at all times.

11.21. SYMBOLS USUALLY EMPLOYED FOR CURRENTS AND VOLTAGES IN TRANSISTOR APPLICATIONS

Usually, the symbols shown in the following table are employed for currents and voltages in transistor applications :

S. No.	*Particulars*	*Instantaneous a.c. values*	*d.c. values*	*Total or resultant values*
1.	Emitter current	i_e	I_E	i_E
2.	Collector current	i_c	I_C	i_C
3.	Base current	i_b	I_B	i_B
4.	Collector-emitter voltage	v_{ce}	V_{CE}	v_{CE}
5.	Emitter-base voltage	v_{eb}	V_{EB}	v_{EB}

11.22. TRANSISTOR LOAD LINE ANALYSIS

Before applying a transistor, the transistor circuit is generally required to be analysed *i.e.* for a given collector-emitter voltage we must know the value of collector current. This can be obtained by plotting the

*Here sine wave is considered as a signal because it is convenient for testing the amplifiers. However, in actual practice, the signal may be a speech on music etc., which is a complex wave having little resemblance to a sine wave. But according to fourier series analysis, all these complex waves are the sum of a number of sine waves of different frequencies. Hence, sine wave in considered as a signal.

output characteristics and then determining the collector current at a desired collector-emitter voltage. However, the solution of such problems can be obtained more easily and frequently by using the method known as *load line analysis method.*

DC Load line

Consider a CE *npn* transistor circuit shown in Fig. 11.27, where no signal is applied to the input side. For this circuit d.c. conditions will prevail and the output characteristics of such a circuit are shown in Fig. 11.28.

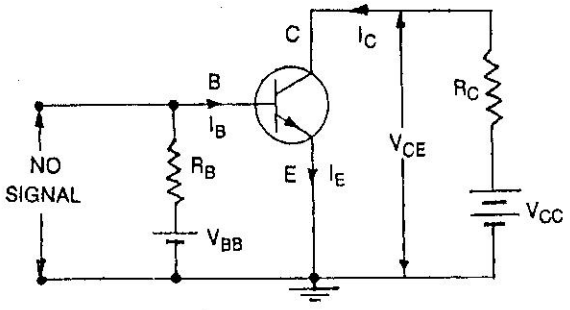


Fig. 11.27.

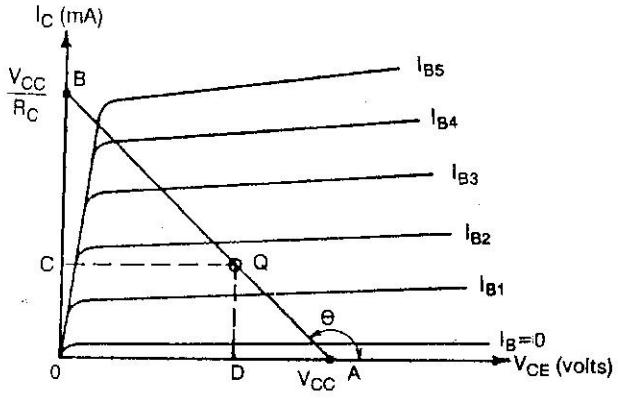


Fig. 11.28.

Applying Kirchhoff's voltage law to the collector circuit, we get,

$$V_{CC} = V_{CE} + I_C R_C$$

or
$$V_{CE} = V_{CC} - I_C R_C \quad ...(i)$$

In the above equation, V_{CC} and R_C are the fixed values (constants), therefore, it is a first degree equation and can be represented by a *straight line on the output characteristics. This line is known as *dc* ***load line,* when it is added to the output characteristics, it is used to determine the locus of V_{CE} and I_C points for a given value of R_C. The two end points of the load line are located as under :

(*i*) The collector-emitter voltage V_{CE} will be maximum, when collector current $I_C = 0$, then, from equation (*i*), we get,

$$V_{CE} = V_{CC} - 0 \times R_C$$

i.e.
$$V_{CE} = V_{CC} \quad ...(ii)$$

This gives first point A ($OA = V_{CC}$) on the collector-emitter voltage axis as shown in Fig. 11.28.

(*ii*) The collector current I_C will be maximum, when collector-emitter voltage $V_{CE} = 0$, then from equation (*i*), we get,

$$O = V_{CC} - I_C R_C$$

or
$$I_C = \frac{V_{CC}}{R_C}$$

This gives second point B ($OB = V_{CC}/R_C$) on the collector current axis as shown in Fig. 11.28.

By joining the two points A and B, d.c. load line is drawn (See Fig. 11.28).

---

*$V_{CE} = V_{CC} - I_C R_C$

or
$$I_C = \left(-\frac{1}{R_C}\right) V_{CE} + \frac{V_{CC}}{R_C} \text{ where } \left(-\frac{1}{R_C}\right) \text{ and } \left(\frac{V_{CC}}{R_C}\right) \text{ are the constants}$$

Hence, the above equation can be compared with the standard equation of a straight line *i.e.* $y = mx + c$.

**As the inclination of the line depends upon R_C *i.e.* load resistance, hence the name *load line.*

With the help of load line, for any value of collector current OD, the value of $V_{CE}(= OC)$ can be determined as shown in Fig. 11.28.

11.23. OPERATING POINT

The point obtained by the values of I_C and V_{CE} when no signal is applied at the input is known as **operating point.**

It is called an operating point since variation of I_C and V_{CE} takes place around this point when signal is applied at the input. This point is also called *quiescent (silent) point* or simply **Q-point** because it is a point on $I_C - V_{CE}$ characteristics when the transistor is silent *i.e.* no signal at the input. The operating point can be determined very easily by d.c. load line method and is explained below :

For example, it is required to determine the operating point at a particular base circuit current I_{B_1} (say 10 μA). Then as per the circuit conditions d.c. load line $\left(\text{i.e. } OA = V_{CE} = V_{CC} \text{ and } OB = I_C = \frac{V_{CC}}{R_C}\right)$ is drawn on the output characteristics (See Fig. 11.29). The point Q, where the d.c. load line intersects the output characteristic curve $I_{B1} = 10$ μA is the operating point. In the absence of input signal,

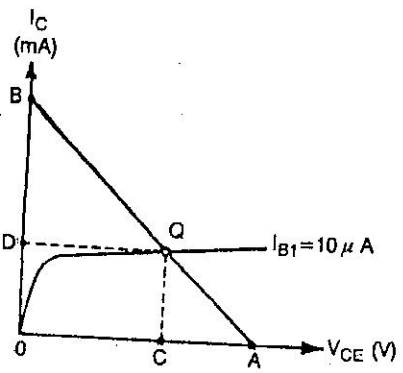


Fig. 11.29.

$$I_C = OD \text{ mA}$$

and

$$V_{CE} = OC \text{ volts}$$

Example 11.13. *A CE circuit of a transistor is shown in Fig. 11.30. Draw the d.c. load line for this circuit.*

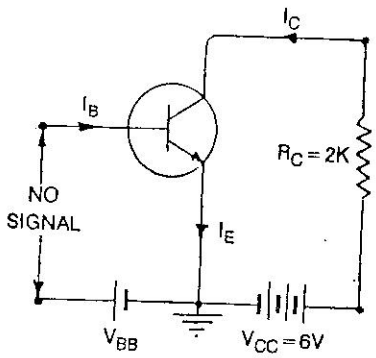


Fig. 11.30.

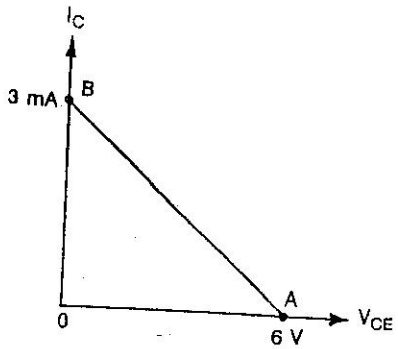


Fig. 11.31.

Sol. The collector-emitter voltage V_{CE} is taken on the x-axis and the collector current I_C is taken on the y-axis as shown in Fig. 11.31.

We know

$$V_{CE} = V_{CC} - I_C R_C$$

To locate point A of the load line on collector-emitter voltage axis, put $I_C = 0$,

Then

$$V_{CE} = V_{CC} = \mathbf{6\ V\ (Ans.)}$$

To locate point B of the load line on collector current axis, put $V_{CE} = 0$,

Then

$$O = V_{CC} - I_C R_C$$

or

$$I_C = \frac{V_{CC}}{R_C} = \frac{6 \text{ V}}{2 \text{ K}} = \mathbf{3\ mA\ (Ans.)}$$

12
Transistor Biasing

INTRODUCTION

The foremost function of a transistor* is to do amplification (*i.e.*, amplitude of a weak signal is amplified). Usually, a weak signal is given to the base circuit of a transistor and an amplified output is obtained at the collector. While doing amplification, care is to be taken that the shape of the signal must remain the same. This amplification of the signal without the change in its shape is known as *faithful amplification.*

In order to achieve faithful amplification, we have to provide some means by which the emitter-base junction is kept in forward-biased and the collector-base junction is kept in the reverse-biased condition during all parts of the signal. This is known as *transistor biasing.*

In fact, to obtain faithful amplification, the *quiescent* (*Q*) point is set usually in the middle of the dc load line. To achieve this some means (circuitry) are provided known as *transistor biasing.* In this chapter, we shall discuss the various methods of providing transistor biasing.

12.1. FAITHFUL AMPLICATION

The process by which, the strength of a weak signal is raised without changing its general shape is known as **faithful amplication.**

The key factor to achieve faithful amplification is to keep the emitter junction in forward-biased and the collector junction in the reverse-biased condition during all parts of the signal. This can be ensured by satisfying the following basic conditions :

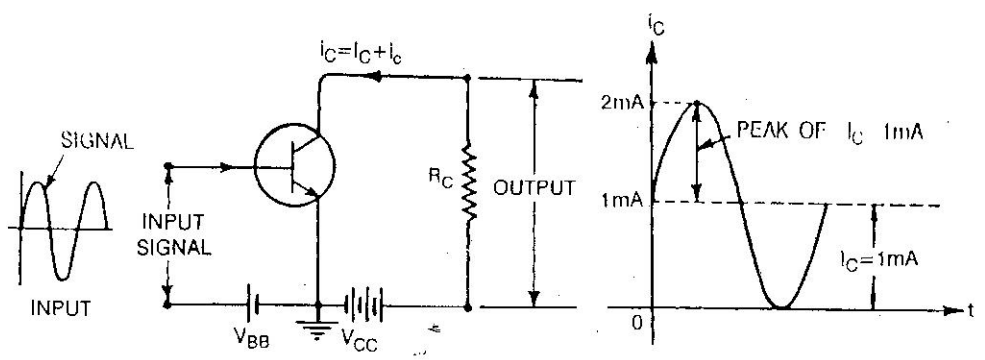
(*i*) Minimum zero signal collector current

(*ii*) Minimum base-emitter voltage

(*iii*) Minimum collector-emitter voltage.

The first two conditions [(*i*) and (*ii*)] ensure that the emitter-base junction is forward-biased during all parts of the signal, whereas, the third condition ensures that the collector-base junction is reverse-biased at all the times.

(*i*) **Minimum zero signal collector current :** When no signal is applied at the input, the current flowing



(*a*) (*b*)

Fig. 12.1.

*A transistor amplifier circuit is a linear circuit since the circuit is used as a current source another example of linear circuit is an *LED* is derived with a transistor. However, when a transistor is used as a switch in any circuit, it is called a digital circuit.

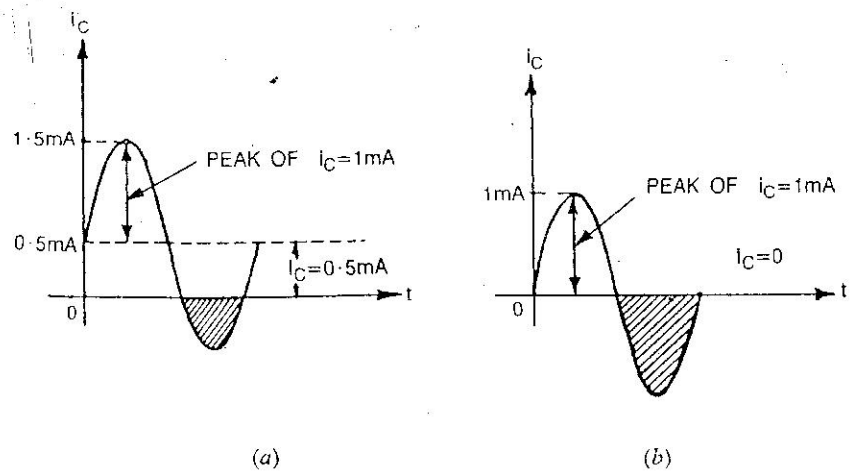
through the collector is known as zero signal collector current (I_C). For fa hfull amplification, the value of zero signal collector current must be more than or equal to the peak value of collector current due to signal alone, *i.e.*

Zero signal collector current $\geq$ peak value of collector current due to signal alone

$$I_C \geq i_c \text{ (peak)}$$

Illustration : Consider a circuit shown in Fig. 12.1. When no signal is applied, a dc current I_C will flow in the collector circuit due to V_{BB}. This collector current is known as zero signal collector current I_C (say its value is 1 mA).

Now, suppose a signal is applied to the input circuit which gives a peak collector current of 1 mA. In this case, during positive half-cycle of the signal, the input circuit is more forward biased and hence the collector current increases, whereas, during negative half-cycle, the input circuit is less forward biased and the collector current decreases. However, a complete amplified signal is obtained at the output, as shown in Fig. 12.1 (*b*). This is because $I_C = i_c$ (peak value).



(*a*) (*b*)

Fig. 12.2.

Now, consider a circuit in which zero signal collector current is set at 0.5 mA (*i.e.* $I_C = 0.5$ mA). If the same signal is applied at the input which produces a peak collector current of 1 mA. Then some part of the negative half-cycle of the signal will be cut off (shown by shaded portion in Fig. 12.2 (*a*) and a distorted signal is obtained at the output.

If the zero signal collector current is set at zero (*i.e.* $I_C = 0$) then complete negative-half-cycle of the signal will be cut off as shown in Fig. 12.2 (*b*).

Thus, it is concluded that to obtain faithful amplification, the zero collector current I_C must be set equal to or more than the peak of collector current due to signal only.

(*ii*) **Minimum base-emitter voltage :** In order to achieve faithful amplification, the potential barrier at the base-emitter junction must be wiped off. The value of potential barrier for Si transistor is 0.7 V and for Ge transistor it is 0.3 V. Therefore, the base-emitter voltage V_{BE} should not fall below 0.7 V for Si and 0.3 V for Ge

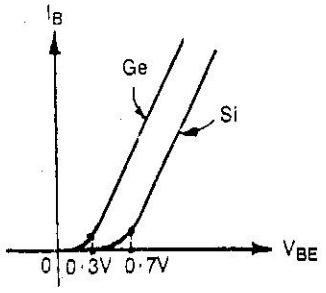
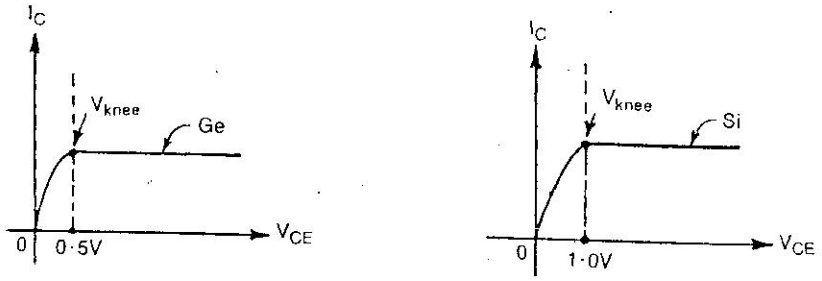


Fig. 12.3.

transistor. In fact, the base current I_B is very small until the *input voltage overcomes the potential barrier at the base-emitter junction. Once the potential barrier is overcome, the base current and hence the collector current increases quickly (See Fig. 12.3).

However, if at any part of the signal, the base-emitter voltage falls below the above-said values, then that part of the signal will not be amplified to the required extent and there will be distortion in the amplified signal.

(*iii*) **Minimum collector-emitter voltage.** In order to achieve faithful amplification, the collector-emitter voltage V_{CE} should not fall below 1.0 V for Si transistor and 0.5 V for Ge transistor, called *knee voltage* (See Fig. 12.4).



(*a*) (*b*)

Fig. 12.4.

When the value of V_{CE} falls below the above-said values, the collector junction will not be properly reverse biased. Therefore, the collector will not be able to attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base. This decreases the collector current while the base current increases. Hence, the value of β-falls.

Hence, if the value of V_{CE} falls below V_{knee} during any part of the signal, that part will be less amplified due to reduced β. Thus, a distorted output signal is obtained.

12.2. TRANSISTOR BIASING

The process by which the required conditions such as proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal are obtained is known as **transistor biasing.**

The basic purpose of transistor biasing is to keep the emitter junction forward-biased and the collector junction properly reverse biased during the application of signal so that faithful amplification can be achieved. The biasing can be achieved either by using bias batteries V_{BB} and V_{CC} or by applying associating circuitry with the transistor. Generally, the latter method is employed since it is more efficient.

The circuitry which provides the necessary conditions of transistor biasing in known as **biasing circuit.**

In fact, a transistor biasing sets up the quiescent point Q (or operating point) on the d.c. load line.

12.3. SELECTION OF OPERATING POINT

While designing a biasing circuit, various transistor ratings such as maximum collector current $I_{C\,(max.)}$, maximum collector-emitter voltage $V_{CE\,(max.)}$ etc. are kept in view for safe operation of the transistor. In the amplifier circuits, a load resistance R_C is connected in the collector circuit. Then a d.c. load line AB corresponding to this resistance R_C is drawn on the output characteristics as shown in Fig. 12.5. The operating point will lie somewhere on this load line. Depending upon the base current, the operating point may lie at C, D or E.

*In actual practice, a.c. signals applied at the input have small voltage level (< 0.1 V) and if they are applied directly, they will not be in position to drive any collector current.

Sol. Here $V_{CC} = 9$ V ; $R_C = 4$ kΩ

(*i*) For faithful amplification, $V_{CE} = 1$ V for silicon transistor.

$\therefore$ Maximum voltage allowed across $R_C = 9 - 1 = 8$ V

$$\text{Maximum allowed collector current} = \frac{8 \text{ V}}{4 \text{ k}\Omega} = 2 \text{ mA}$$

The maximum collector current should not be allowed to rise above this value otherwise it will result in unfaithfull amplification.

(*ii*) When the signal is applied, the collector current can at the most be allowed to fall to zero during the negative peak of the signal.

$\therefore$ Zero signal collector current, $I_C = \frac{2 \text{ mA}}{2} = 1$ mA

At positive peak of the signal, $i_C = I_C + i_c = 1 + 1 = 2$ mA

At negative peak of the signal, $i_C = 1 - 1 = 0$

(*iii*) Peak value of the signal collector current = 1 mA

Peak value of the signal base current, $i_B = \frac{i_C}{\beta} = \frac{1 \text{ mA}}{50} = 20$ μA ($\because \quad i_C = \beta i_B$)

12.4. INHERENT VARIATIONS OF TRANSISTOR PARAMETERS

Inspite of tremendous advancement in semiconductor technology, the transistor parameters (such as β and V_{BE}) vary between wide limits even among different units of the same type. For example, 2N3054 is an *npn* general purpose power transistor having β-25 to 100 *i.e.* β for one transistor may be 25 and for the other it may be 100, although both of them are 2N3054 transistors. Similarly BC 147 is a silicon *npn* transistor having β 100 to 600. This inherent variation in the transistor parameters of the same type is because it is not possible to control the base width with the present semiconductor technology. A minute variation in the base width changes its parameters.

The inherent variations of transistor parameters may change the operating point, resulting in unfaithful amplification (*i.e.* distorted output signal). Therefore, while designing the biasing circuit, this property of transistors is taken into consideration. The biasing circuit is designed which can work with all the transistors of one type whatever may be the value of β or V_{BE}.

12.5. STABILISATION

The quiescent point or operating point is represented by zero signal collector current I_C and V_{CE}. If either of the two changes, the operating point is shifted.

Causes of unstabilisation. An amplifier or transistor is said to be unstabilised when its operating point is shifted. Generally, it occurs because of the change in collector current. The collector current in a transistor changes rapidly when

(*i*) the temperature changes (it affects I_C).

(*ii*) the transistor is replaced by another one of the same type. This is due to the inherent variations of transistor parameters (*i.e.* β).

Effect of temperature on I_C. The collector current is given by the relation ;

$$I_C = \beta I_B + I_{CEO} \text{ where } I_{CEO} = (\beta + 1)\ I_{CBO}$$

$\therefore$
$$I_C = \beta I_B + (\beta + 1) I_{CBO} \qquad ...(i)$$

The collector leakage current I_{CBO} is greatly influenced by the temperature. Under working conditions, the flow of collector current produces heat within the transistor. This raises the temperature of the transistor and increases I_{CBO}. This in turn increases the collector current I_C as $I_C = \beta I_B + (\beta + 1)\ I_{CBO}$. The rise in

collector current further increases the temperature resulting in further increase in I_{CBO}. Such a cumulative effect leads to thermal runway.

The self-destruction of an unstabilised transistor due to rise in temperature is called **thermal runway.**

Effect of inherent variations of transistor parameters. When a transistor is replaced by another of the same type, that may have different parameters. Since collector current $I_C = \beta I_B + (\beta + 1)\, I_{CBO}$, the value of I_C will be different if the new transistor having different value of β is applied. Hence the inherent variations of transistor parameters shift the operating point when it is not properly stabilised.

Need of stabilization

In order to avoid thermal runway (*i.e.* self-destruction of transistor because of rise in temperature) and to nullify the effect of inherent variations of transistor parameters, it is very essential to stabilise the operating point *i.e.* to fix the operating point at all conditions. In practice, it is done by selecting a suitable biasing circuit which decreases I_B automatically with the rise in temperature (or rise in β while replacing the transistor). Then decrease in βI_B will compensate for the increase in $(\beta + 1)\, I_{CBO}$, keeping I_C nearly constant. Hence, the associated circuitry can be applied to stabilise the operating point in the transistors.

Thus **stabilisation** may be defined as ;

The process of making operating point independent of temperature changes or inherent variations in transistor parameters is called **stabilisation.**

12.6. REQUIREMENTS OR ESSENTIALS OF A TRANSISTOR BIASING CIRCUIT

From the discussions in the above sections, it may be summarized that transistor biasing is required for faithful amplification. The biasing circuit should meet the following requirement :

(*i*) It should ensure proper zero signal collector current and V_{CE} *i.e.* it should establish the operating point in the centre of the active region of the characteristics, so that the signal may not cut off at any part.

(*ii*) It should ensure that V_{CE} does not fall the required limits (*i.e.* 1.0 V for *Si* and 0.5 V for *Ge* transistors).

(*iii*) It should ensure the stabilisation of collector current against temperature variations.

(*iv*) It should ensure to make the operating point independent of transistor parameters.

12.7. STABILITY FACTOR

It has already been discussed that the stability of the operating point means the value of I_C remains constant even though there is variation in I_{CBO} (or I_{CO}) because of rise in temperature. The extent to which a biasing circuit achieves this goal is measured by the *stability factor.* It may be defined as under :

The rate of change of collector current I_C w.r.t. the rate of change of collector leakage current I_{CBO} (or I_{CO}) at constant I_B and β is called **stability factor.**

i.e. Stability factor, $$S = \frac{dI_C}{dI_{CO}} \text{ at constant } I_B \text{ and } \beta$$

In fact, the stability factor shows the change in collector current I_C because of the change in collector leakage current I_{CO}. The lower the value of stability factor, greater is the thermal stability of the transistor. The ideal value of stability factor is 1 but it is never achieved in practice. However, the values of S below 25 results in satisfactory performance.

General expression of stability factor for CE configuration. The collector current is expressed as :

$$I_C = \beta I_B + (\beta + 1)\, I_{CO}$$

Differentiating the above expression w.r.t. I_C, we get

$$1 = \beta \frac{d}{dI_C} I_B + (\beta + 1) \frac{d}{dI_C} I_{CO} = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{dI_C/dI_{CO}} = \beta \frac{dI_B}{dI_C} + \frac{(\beta + 1)}{S}$$

or $$\frac{(\beta + 1)}{S} = 1 - \beta \frac{dI_B}{dI_C}$$

or $$S = \frac{\beta + 1}{1 - \beta \dfrac{dI_B}{dI_C}}$$

12.8. METHODS OF TRANSISTOR BIASING

So far, in the various transistor amplifier circuits, the biasing was done by applying two batteries V_{BB} in the input and V_{CC} in the output circuit. However, in the interest of simplicity and economy, this biasing arrangement is never applied in the actual circuits.

In actual practice, a single source of supply (V_{CC}) is employed with the necessary biasing circuitry. The basic principle of the biasing circuitry is to obtain the required value of I_B (and hence I_C) from V_{CC} in the zero signal conditions. At the same time the value of collector load resistor R_C is selected such that V_{CE} should never fall below 1 V for silicon and 0.5 V for germanium transistors.

The following are the most commonly used biasing arrangements employing single supply source :

(*i*) Base resistor biasing (*ii*) Feedback resistor biasing

(*iii*) Emitter resistor biasing (*iv*) Voltage divider biasing.

12.9. BASE RESISTOR BIASING

The base resistor biasing for an *npn* transistor is shown in Fig. 12.11. Here, a high resistance R_B (of several hundred kΩ) is connected between the *positive end of the supply and the base. The required zero signal base current I_B is provided by V_{CC}. The supply also keeps the base positive w.r.t. emitter and hence makes the base-emitter junction forward biased.

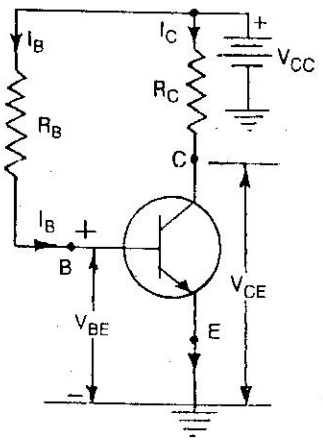


Fig. 12.11.

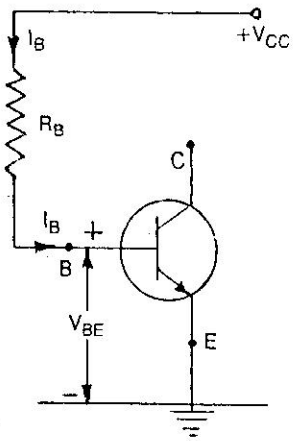


Fig. 12.12.

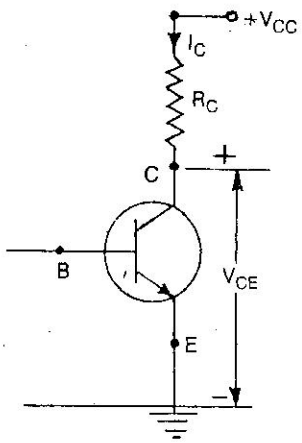


Fig. 12.13.

Circuit analysis. While analysing the circuit, generally we make the equations to determine the value of R_B for the required zero signal collector current. Let I_C be the required zero signal collector current. Then

$$I_B = \frac{I_C}{\beta} \qquad ...(i) \text{ (since } I_C = \beta I_B)$$

*In case of *pnp* transistor, the negative end of the supply is connected to the collector through R_c and resistor R_B is connected between –ve end of the supply and base.

Considering only the input circuit shown in Fig. 12.12 and applying Kirchhoff's voltage law (*KVL*) to the base-emitter loop, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

or $$I_B R_B = V_{CC} - V_{BE}$$

or $$R_B = \frac{V_{CC} - V_{BE}}{I_B} \quad ...(ii)$$

The value of R_B can be determined from the exp. (*ii*) as the values of V_{CC} and I_B are known and V_{BE} can be seen from the transistor manual.

Since the value of V_{BE} is quite small as compared to V_{CC}, it is generally neglected to simplify the expression. Then

$$R_B \cong \frac{V_{CC}}{I_B}$$

It may be noted that V_{CC} is a fixed known value and I_B is fixed by the operating conditions, therefore, this biasing method is sometimes called *fixed biasing method.*

As the operating point is represented by I_C ; V_{CE}, therefore, for the selected value of I_C, we have to determine the value of V_{CE}. For this consider only the output circuit shown in Fig. 12.13.

Applying Kirchhoff's voltage law (*KVL*) to the collector-emitter loop, we get,

$$V_{CC} = I_C R_C + V_{CE}$$

or $$V_{CE} = V_{CC} - I_C R_C \quad ..(iii)$$

Stability factor : It is given by the exp.

$$S = \frac{\beta + 1}{1 - \beta \dfrac{dI_B}{dI_C}}$$

In this biasing arrangement, I_B is independent of I_C. Therefore $dI_B/dI_C = 0$. Substituting this value in the above exp., we get,

$$S = \beta + 1$$

Thus, the value of stability factor in fixed biasing method is very high which shows its poor thermal stability.

Advantages

(*i*) In this biasing method, calculations are simple and it is easy to obtain the required conditions.

(*ii*) Simple in construction as only one resistor R_B is required to set the conditions.

(*iii*) There is no loading of the source as no resistor is employed across base-emitter junction.

Disadvantages

(*i*) It provides poor thermal stability (high stability factor) and there are chances of thermal runway.

(*ii*) This method provides poor stability against inherent variations of transistor parameters. For instant, if β increases due to transistor replacement, then I_C also increases by the same factor as $I_C = \beta I_B$ where I_B is constant.

In fact, in this biasing arrangement no means are provided to check a self increase in collector current due to temperature rise and individual variations. Due to these disadvantages, this method is rarely employed is practical circuits.

Example 12.2. *A base resistor biasing circuit is shown in Fig. 12.14. Determine (i) the collector current I_C and collector-emitter voltage V_{CE}. Neglect small V_{BE} and assume $\beta = 60$. (ii) If R_B in this circuit is changed to 200 kΩ and transistor is considered to be silicon npn.*

Also neglecting V_{BE},

$$R_B = \frac{V_{CC}}{I_B} = \frac{6}{80\ \mu A} = 75\ k\Omega$$

$$\% \text{ error} = \frac{75 - 73.15}{73.15} \times 100 = \mathbf{2.529\ \%} \quad \textbf{(Ans.)}$$

Comments : This error is too small and should not be bothered at all. Moreover the resistors available in the market ordinarily have tolerance ±10%. Hence, it is not very incorrect to neglect V_{BE} and I_{CBO} while doing calculations.

When β changes to 40 and I_{CBO} to 10 μA due to rise in temperature ;

$$I_C = \beta I_B + (\beta + 1)I_{CBO} = 40 \times 77.92\ \mu A + (40 + 1) \times 10\ \mu A$$
$$= 3116.8 + 410 = 3526.8\ \mu A = \mathbf{3.527\ mA} \quad \textbf{(Ans.)}$$

Comments : It may be noted that the collector current has increased by more than 50% due to change in parameters by the rise in temperature. Hence, it is concluded that the operating point is shifted due the rise in temperature in this biasing circuit.

12.10. FEED BACK RESISTOR BIASING

The feed back resistor biasing is also known as collector to base resistor biasing. This biasing arrangement for an *npn* transistor is shown in Fig. 12.20. Here, a high resistance R_B is connected between collector and base. The required zero signal base current is determined by collector-base voltage V_{CB} and not by V_{CC}. Hence, the base-emitter junction is forward biased and base current I_B flows through R_B. This in turn causes the zero signal collector current I_C to flow in the circuit.

It may be noted that the collector (output) is connected to the base (input) through R_B. This means that feedback exists in the circuit. The base current depends upon the collector voltage. That is why this circuit is also called a voltage feedback biasing circuit.

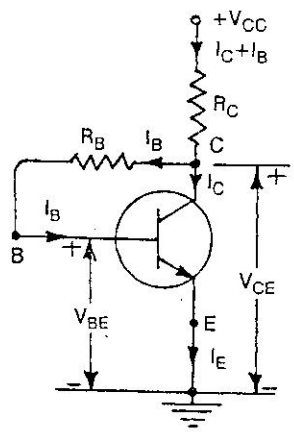


Fig. 12.20.

Circuit analysis

While analysing the circuit, generally we make the equations to determine the value of R_B for the required zero signal collector current I_C.

Referring Fig. 12.20, the loop equation for the input circuit is

$$V_{CC} = R_C(I_C + I_B) + I_B R_B + V_{BE} \quad ...(i)$$

or $$V_{CC} = I_C R_C + I_B(R_C + R_B) + V_{BE}$$

or $$I_B(R_C + R_B) = V_{CC} - I_C R_C - V_{BE}$$

or $$R_B = \frac{(V_{CC} - I_C R_C) - V_{BE}}{I_B} - R_C \quad ...(ii)$$

Writing loop equation for the output circuit, we get

$$V_{CC} = V_{CE} + (I_C + I_B)R_C \quad ...(iii)$$

or $$V_{CE} \cong V_{CC} - I_C R_C \quad \text{(neglecting } I_B \text{ since } I_B << I_C\text{)}$$

Substituting this value in eqn. (*ii*), we get,

$$R_B = \frac{V_{CE} - V_{BE}}{I_B} - R_C \simeq \frac{V_{CE} - V_{BE}}{I_B} \quad ...(iv) \text{ (since } R_C << R_B\text{)}$$

$$= \frac{V_{CE}}{I_B} \quad \text{where} \quad I_B = \frac{I_C}{\beta}$$

For determining the operating point, consider eqn. (*i*) and put $I_C = \beta I_B$, we get.

$$V_{CC} = \beta I_B R_C + I_B(R_C + R_B) + V_{BE}$$

or $$V_{CC} = I_B[R_B + (\beta + 1)R_C] + V_{BE}$$

or $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_C} \cong \frac{V_{CC}}{R_B + \beta R_C} \quad ...(v)$$

For determining V_{CE}, consider eqn. (*iii*) ;

$$V_{CC} = V_{CE} + (I_B + I_C)R_C$$

or $$V_{CE} = V_{CC} - (I_B + I_C)R_C \cong V_{CC} - I_C R_C \quad ...(vi)$$

Stability factor. The stability factor of this type of biasing arrangement is less than $(\beta + 1)$, *i.e.*

$$S < (\beta + 1)$$

Advantages

(*i*) It is a simple biasing arrangement as only one resistor R_B is required.

(*ii*) This biasing circuit provides some stabilisation of the operating point as explained below :

Suppose temperature increases, this causes increase in leakage current and at the same time there is increase in β due to inherent variation in parameters. This increases the collector current since $I_C = \beta I_B + (\beta + 1)I_{CBO}$. As the collector current increases, the voltage V_{CE} decreases as $V_{CE} = V_{CC} - I_C R_C$. The decrease in V_{CE} causes decrease in base current since $I_B = \frac{V_{CE} - V_{BE}}{R_B}$ [*see* eqn. (*iii*)]. This decrease in base current in turn decreases the collector current to bring it to original value. Hence, there is a tendency of this circuit to stabilise the operating point.

Disadvantages

(*i*) The stability factor of this biasing method is quite high. Hence, the operating point does change, although to lower extent, due to temperature rise or inherent variations in parameters.

(*ii*) The resistor R_B not only provides dc feedback for stabilisation of operating point, but it also causes ac feedback. This reduces the voltage gain of the amplifier which is not desirable. *Because of this drawback, this circuit is* **seldom used in operational amplifiers.**

Example 12.7. *Determine the emitter current and collector voltage V_C in the circuit shown in Fig. 12.21. Comment on the results.*

Sol. The loop equation for the input circuit is,

$$V_{CC} = (I_C + I_B)R_C + I_B R_B + V_{BE} = I_C R_C + I_B(R_C + R_B) + V_{BE}$$
$$= \beta I_B R_C + I_B(R_C + R_B) + V_{BE} = I_B[(\beta + 1)R_C + R_B] + V_{BE}$$

or $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_C} \cong \frac{V_{CC}}{R_B + \beta R_C} \quad \text{(neglecting } V_{BE}\text{)}$$

Here, $V_{CC} = 12$ V ; $R_B = 600$ kΩ ; $\beta = 100$

and $R_C = 600\ \Omega = 0.6$ kΩ

$$\therefore \quad I_B = \frac{12\ V}{600\ \text{k}\Omega + 100 \times 0.6\ \text{k}\Omega} = \frac{12\ V}{660\ \text{k}\Omega} = 18.18\ \mu\text{A}$$

Collector current, $I_C = \beta I_B = 100 \times 18.18 = 1818\ \mu\text{A} = 1.818$ mA

Emitter current, $I_E = I_C + I_B \cong I_C = \mathbf{1.818\ mA}$ **(Ans.)**

Collector voltage, $V_C = V_{CE} = V_{CC} - I_C R_C = 12 - 1.818\ \text{mA} \times 0.6\ \text{k}\Omega$

$= 12 - 1.09 = \mathbf{10.91\ V}$ **(Ans.)**

Comments : It may be noted that $V_{CE} = 10.91$ V which is slightly less than V_{CC}. Hence the operating (quiescent) point in very near to the cut-off region.

have been base bias resistor circuit then collector current would have been increased to four times. Hence, this method of biasing in better than the base bias resistor method.

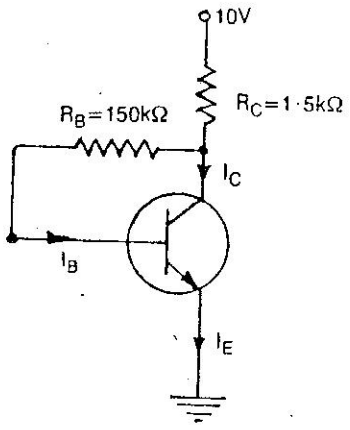


Fig. 12.23.

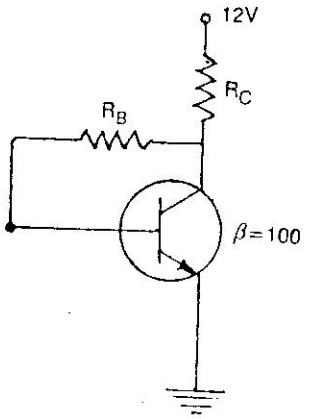


Fig. 12.24.

Example 12.10. *It is desired to set the operating point using feedback resistor method of biasing at I_C = 1 mA ; V_{CE} = 8 V. What will be the value of R_C and R_B if V_{CC} = 12 V, V_{BE} = 0.3 V and β = 100 ?*

(ii) *What will be the new operating point if β changes to 150 assuming all other values for the circuit to be the same ?*

Sol. The required feedback resistor biasing circuit is shown in Fig. 12.24.

$$V_{CC} = V_{CE} + I_C R_C$$

$$\therefore \quad R_C = \frac{V_{CC} - V_{CE}}{I_C} = \frac{12 - 8}{1 \text{ mA}} = \mathbf{4\ k\Omega\ (Ans.)}$$

Also, $$I_B = \frac{I_C}{\beta} = \frac{1 \text{ mA}}{100} = 0.01 \text{ mA}$$

Using simple relation

$$R_B = \frac{V_{CE} - V_{BE}}{I_B} = \frac{8 - 0.3}{0.01 \text{ mA}} = \mathbf{770\ k\Omega\ (Ans.)}$$

(*ii*) If β changes to 150

Base current, $$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta R_C} = \frac{12 - 0.3}{770 \text{ k}\Omega + 150 \times 4 \text{ k}\Omega} = 8.54\ \mu\text{A}$$

Collector current, $I_C = \beta I_B = 150 \times 8.54\ \mu\text{A} = 1.281$ mA

Collector emitter voltage,

$$V_{CE} = V_{CC} - I_C R_C = 12 - 1.281 \text{ mA} \times 4 \text{ k}\Omega = 6.876 \text{ V}$$

The new operating point is **6.876 V, 1.281 mA (Ans.)**

Comments : The results show that this biasing arrangement does not provide the required stabilisation.

12.11. EMITTER RESISTOR BIASING

The emitter resistor biasing for an *npn* transistor is shown in Fig. 12.25. It is just a modification to the base resistor biasing circuit. In this biasing an additional resistor R_E is connected in the emitter. Hence this circuit contains three resistors R_B, R_E and R_C.

Circuit analysis

The circuit may be analysed for determining the operating point Q. To do this, equations can be framed for the input and output circuits.

Writing the loop equation for the input circuit, we get,

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

or $$V_{CC} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E$$

[since $I_E = (\beta + 1) I_B$]

or $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E}$$

Neglecting V_{BE} since it is very small

or $$I_B \cong \frac{V_{CC}}{R_B + \beta R_E} \quad ...(i)$$

Collector current, $I_C = \beta I_B = \frac{\beta V_{CC}}{R_B + \beta R_E} = \frac{V_{CC}}{R_E + R_B/\beta}$ ...(ii)

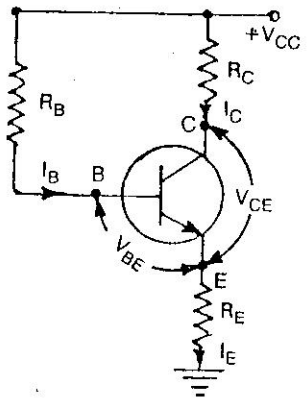


Fig. 12.25.

Writing the loop equation for the output circuit, we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

or $$V_{CE} = V_{CC} - (R_C + R_E) I_C \qquad (\because I_C \cong I_E) \qquad (iii)$$

Thus, the operating point can be obtained by using eqn. (*ii*) and (*iii*).

Similarly, for the given operating point, the value of R_B and R_E can be determined by using eqn. (*ii*) and (*iii*) provided the other data *viz* V_{CC}, R_C and β are known.

Stabilisation

Let us see the effect of increase in temperature on the operating point Q. For this rewrite the loop equation for input circuit ;

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

or $$I_B = \frac{V_{CC} - I_E R_E - V_{BE}}{R_B}$$

or $$I_B \cong \frac{V_{CC} - I_E R_E}{R_B} \qquad \text{(since } V_{BE} \text{ is very small)} \qquad (iv)$$

As the temperature increases, the leakage current increases. This increases the collector current I_C as well as emitter current I_E. As a result voltage drop $I_E R_E$ increases which reduces the numerator of equation (*iv*) and hence the current I_B reduces. This results in reduction of collector current. Thus, an increase in collector current is brought back to its previous value by the sequence of events. Hence, the stability of the operating point is improved to large extent by inserting a resistor in the emitter circuit.

The stabilisation is improved by inserting R_E in the emitter circuit. This resistor is present in the output side as well as the input side. Therefore, a feedback occurs through this resistor. The feedback voltage is proportional to the emitter current I_E. Hence, the circuit is also called *current feedback biasing*, circuit.

Stability factor. The stability factor of this type of biasing circuit is quite less than $(\beta + 1)$.

Advantages

(*i*) Although three resistors R_C, R_B and R_E are employed in the circuit, still it is quite simple to explain.

(*ii*) It provides far better stabilisation.

Disadvantages

(*i*) The stability factor of this biasing is quite high. Hence, the operating point does change, although to lower extent, due to temperature rise or inherent variations in parameters.

(*ii*) The dc feedback helps in the stabilisation of operating point but at the same time ac feedback reduces the voltage gain of the amplifier. This is an undesirable feature. However, this drawback can be remedied by putting a capacitor C_E across the resistor R_E. The capacitor C_E offers very low impedance to the ac current (signal) and does not allow it to pass through R_E and hence ac feedback is restricted. Thus the process of amplification remains unaffected.

This biasing circuit is also *not used practically* because of the following reasons :

Refer to equation (*ii*) *i.e.*, $I_C = \dfrac{V_{CC}}{R_E + R_B/\beta}$;

For stability, the denominator should be independent of β. It is only possible if $R_E >> \dfrac{R_B}{\beta}$. This condition can only be obtained either using R_E of very large value or by using R_B of very small value. Now, a large value of R_E will cause a large voltage drop across it and to obtain a required Q point we have to apply a voltage source V_{CC} of high value. On the other hand if R_B is of very low value we have to use a separate voltage source of low value for base circuit. Both these alternatives are quite impractical. Hence, this biasing circuit is not used practically.

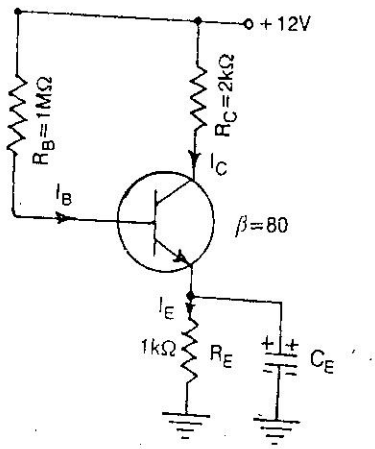


Fig. 12.26.

Example 12.11. *Calculate the values of three currents in the circuit shown in Fig. 12.26.*

Sol. Here, $V_{CC} = 12$ V ; $R_C = 2$ kΩ ;
$R_B = 1$ MΩ = 1000 kΩ ;
$\beta = 80$ and $R_E = 1$ kΩ.

Loop equation for the input circuit

$$V_{CC} = I_B R_B + V_{BE} + I_E R_E$$

where $I_E = I_C + I_B = \beta I_B + I_B = (\beta + 1) I_B$

$\therefore$ $V_{CC} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E$

or $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{V_{CC}}{R_B + (\beta + 1)R_E} \qquad (\because V_{BE} = 0, \text{ neglected})$$

$$= \frac{12\ V}{1000\ \text{k}\Omega + (80 + 1) \times 1\ \text{k}\Omega} = \frac{12\ V}{1081\ \text{k}\Omega} = \mathbf{11.1\ \mu A\ (Ans.)}$$

Collector current, $I_C = \beta I_B = 80 \times 11.1 = \mathbf{888\ \mu A\ (Ans.)}$

Emitter current, $I_E = I_C + I_B = 888 + 11.1 = \mathbf{899.1\ \mu A\ (Ans.)}$

Example 12.12. *Calculate the value of R_B in the biasing circuit shown in Fig. 12.27 so that the operating point is fixed at $I_C = 6.4$ mA and $V_{CE} = 3$ V ; $\beta = 80$.*

Sol.

Base current, $$I_B = \frac{I_C}{\beta} = \frac{6.4\ \text{mA}}{80} = 80\ \mu\text{A}$$

Now, $$V_{CC} = I_B R_B + V_{BE} + (\beta + 1) I_B R_E$$

or $$R_B = \frac{V_{CC} - (\beta + 1) I_B R_E}{I_B} \quad \text{neglecting } V_{BE}$$

$$= \frac{10 - (80 + 1) \times 80 \times 10^{-6} \times 500}{80 \times 10^{-6}} = \frac{10 - 3.24}{80 \times 10^{-6}} = \mathbf{84.5\ k\Omega\ (Ans.)}$$

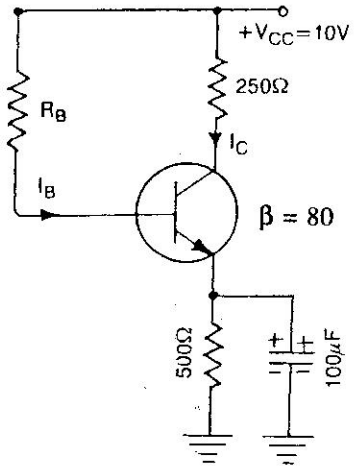


Fig. 12.27.

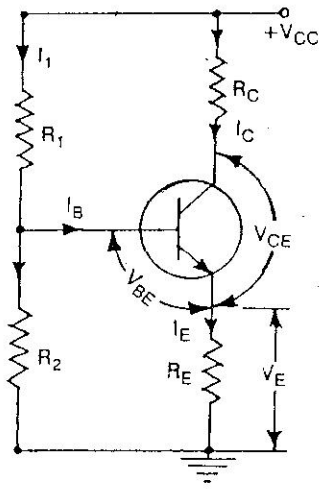


Fig. 12.28.

12.12. VOLTAGE-DIVIDER BIASING

The voltage divider biasing for an *npn* transistor is shown in Fig. 12.28. In this biasing circuit, two resistors R_1 and R_2 are connected across the supply voltage V_{CC} and provide the necessary biasing. Whereas, a resistor connected in the emitter circuit R_E provides stability. Since the resistors R_1 and R_2 form the voltage divider hence the name *voltage divider biasing*. The voltage drop across R_2 forward bias the base-emitter junction and causes the base current. Hence, collector current flows which sets up the zero signal conditions. This is the most widely used method of providing biasing and stabilisation to transistor since the operating point, in this case, can be made almost independent of β (beta).

Circuit analysis

The circuit can be analysed either by using approximations or by accurate method (applying thevenin theorem). Usually, approximate analysis are employed since it provides resonable *accuracy.

Consider the input section of the circuit. Let current I_1 flows through resistors R_1. As the base current I_B is very small, therefore, it can be assumed that same current I_1 flows through the resistors R_2 (*i.e.*, $I_1 \cong I_2 >> I_B$).

Applying Kirchhoff's voltage law to the input circuit, we get,

$$V_{CC} = I_1R_1 + I_1R_2$$

or
$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

Voltage across resistor R_2,

$$V_2 = I_1R_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2 \qquad ...(i)$$

Writing loop equation in base emitter circuit, we get,

$$V_2 = V_{BE} + V_E$$

or
$$V_2 = V_{BE} + I_ER_E \qquad \text{(since } V_E = I_ER_E\text{)}$$

*It will be justified in the examples to follow.

or $$I_E = \frac{V_2 - V_{BE}}{R_E} \quad ...(ii)$$

Since $I_C \cong I_E$

$\therefore$ $$I_C = \frac{V_2 - V_{BE}}{R_E}$$

In all practical circuits $V_2 >> V_{BE}$, therefore, V_{BE} in comparison to V_2 is neglected. Thus

$$I_C = \frac{V_2}{R_E} \quad ...(iii)$$

Applying Kirchhoff's voltage law to the output (collector) side, we get,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

or $$V_{CC} = I_C R_C + V_{CE} + I_C R_E \quad (I_C \cong I_E)$$

or $$V_{CE} = V_{CC} - I_C(R_C + R_E) \quad ...(iv)$$

Stabilisation

In the above analysis, we have seen that β does not appear in any of the expressions. It reveals that the operating point is independent of this parameters (β). It means that if we change the transistor with same type having different value of β, the opperating point will not be affected at all. Hence, a good stabilisation is ensured.

On the other hand, if the collector current increases due to rise in temperature this will cause greater voltage drop across the emitter resistance ($I_C R_E$). As the voltage drop across R_2(*i.e.** V_2) is independent of I_C, therefore V_{BE} decreases (since $V_{BE} = V_2 - I_C R_E$). This in turn causes to decrease I_B. The reduction in I_B restores the original value of collector current I_C.

Stability factor. It can be shown mathematically that the stability factor of this biasing circuit is 1 which is an ideal one. However, in actual practice, its stability factor is around 10.

Advantages

The voltage divider biasing curcuit provides superb stabilisation, therefore, this biasing circuit is invariably employed for transistor biasing.

12.13. THEVENIN ANALYSIS OF VOLTAGE DIVIDER BIASING CIRCUIT

Before analysing the voltage divider biasing circuit of a transistor by Thevenin's theorem, let us have an idea about this theorem. This theorem simply states that a complicated network can be reduced to a voltage source V_{th} in series with a resistor R_{th} across the given pair of terminals AB. Where

V_{th} = The open circuit voltage between the required two terminals A and B called Thevenin voltage, and

R_{th} = The equivalent resistance of the network as seen from the two terminals with all other voltage sources replaced by their internal resistance called Thevenin resistance.

Considering the voltage divider biasing circuit shown in Fig. 12.29. To Thevenise the circuit on the left of the terminals AB, reduce the circuit as shown in Fig. 12.30 to determine the Thevenin voltage V_{th}.

$$V_{th} = \frac{V_{CC}}{R_1 + R_2} \times R_2 = \frac{R_2}{R_1 + R_2} \times V_{CC} \quad ...(i)$$

To determine Thevenin resistance R_{th}, reduce the circuit as shown in Fig. 12.31. Here, R_1 and R_2 are just in parallel, then

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} \quad ...(ii)$$

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*$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$

The resultant Thevenised circuit is shown in Fig. 12.32. Accurate calculations can be made from this circuit as given below :

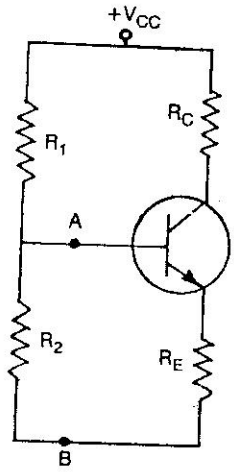

Fig. 12.29.

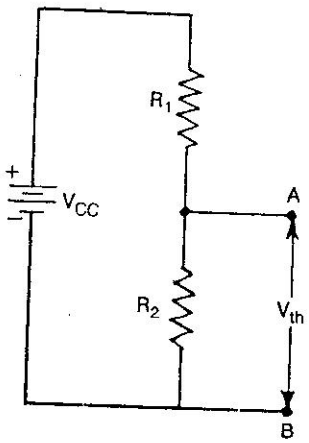

Fig. 12.30.

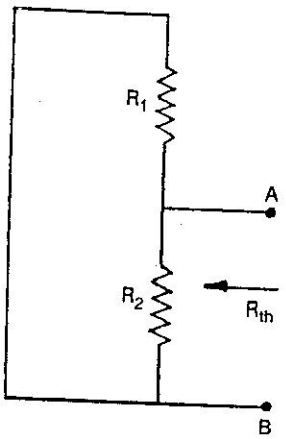

Fig. 12.31.

The loop equation for the input section can be written as

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E \quad ...(iii)$$

or $$V_{th} = I_B R_{th} + V_{BE} + (\beta + 1) I_B R_E$$

$$[\because I_E = (\beta + 1) I_B]$$

or $$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1) R_E} \cong \frac{V_{th}}{R_{th} + \beta R_E} \quad ...(iv)$$

Collector current, $$I_C = \beta I_B = \frac{\beta V_{th}}{R_{th} + \beta R_E} \quad ...(v)$$

The loop equation for the collection circuit can be written as

$$V_{CC} = V_{CE} + I_C R_C + I_E R_F$$

or $$V_{CC} = V_{CE} + I_C R_C + I_C R_E \qquad (\because I_E \cong I_C)$$

or $$V_{CE} = V_{CC} - (R_C + R_E) I_C$$

Although we have made the accurate calculations, but it will be seen in the examples to follow that approximate calculations also yield the same results. Therefore, approximate calculations are usually employed.

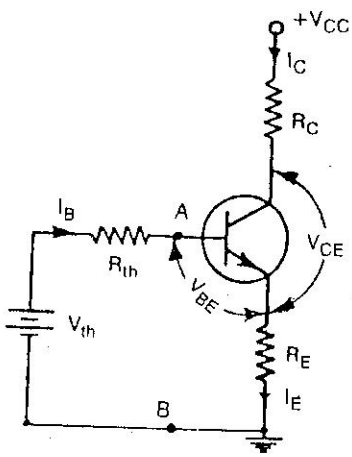

Fig. 12.32.

Example 12.13. *For the circuit shown in Fig. 12.33, draw the dc load line and determine the operating point. Assume V_{BE} = 0.3 V and β = 60 for the transistor used.*

Sol. To draw dc load line, consider the exp.

$$V_{CE} = V_{CC} - I_C (R_C + R_E) \quad ...(i)$$

To locate point A on the collector emitter voltage axis. Put $I_C = 0$ in exp. (i), then

$$V_{CE} = V_{CC} = 12 \text{ V}$$

Hence, $OA = 12$ V

To locate the other point B on the collector current axis put $V_{CE} = 0$ in the exp. (i), we get,

$$0 = V_{CC} - I_C (R_C + R_E)$$