CHAPTER

12 Single Stage Transistor Amplifiers

12.1. INTRODUCTION

One of the most important characteristics of a signal is its amplitude. Sometimes, a signal may have the desired waveform and frequency, and yet cannot be used because of its small amplitude. This is because the circuits or devices, that are to be operated with such signals as their input, need definite levels of amplitude of signal for proper operation. Thus the amplification or strengthening of the input signal becomes imperative. The device that amplifies the input signal is called the *amplifier*.

Almost no electronic system can work without an amplifier. For instance radio receivers amplify very weak signals until they are strong enough to make the sound audible. The transducers employed in medical and scientific investigations generate signals in microvolt or millivolt range which are incapable to operate indicating instruments. So these signals need amplification thousands and million times so as to be strong enough to operate indicating instruments.

We have studied that a properly biased transistor increases the amplitude of a weak signal and so acts as an amplifier. So an amplifier may be defined as a device that increases the current, voltage or power of an input signal with the help of a transistor by furnishing the additional power from a separate source of supply.

When only one transistor with associated circuit is used for increasing the strength of a weak signal, the circuit is known as *single stage transistor amplifier*. It may be emphasised here that a practical amplifier is always a multistage amplifier *i.e.* an amplifier using a number of stages of amplification.

We know that a transistor alone cannot perform the function of amplification and some passive components, such as resistors and capacitors, and a biasing supply is to be connected. When an ac signal is applied between the base and emitter terminals of a properly biased transistor, a small base current starts flowing. Because of transistor action, a much larger ac current (β times the base current) flows through the collector resistor R_C. Since the value of collector resistance is quite high (usually 5–10 kΩ), a large voltage appears across R_C. Thus, a weak signal applied between base and emitter circuit appears in the amplified form between collector and emitter. This explains the *amplifying action of a transistor*. When the input signal is quite weak and produces *small fluctuations* in the collector current in comparison to its quiescent value, the amplifier is called the *small signal amplifier* (or *voltage amplifier*). On the other hand, when the fluctuations produced in collector current are quite large (beyond the linear portion of the output characteristics), the amplifier is called the *large signal* amplifier (or *power amplifier*). Small signal or voltage amplifier is used as the first stage of the amplifier used in radio and TV receivers, tape-recorders, stereos and measuring instruments.

A dc voltage source connected to an amplifier is shown in Fig. 12.1. The amplifier consists of transistors that must be biased in the forward-active region so that the transistors can act as amplifying devices. It is desirable that the output signal is linearly proportional to the input signal so that the output of the speakers is an exact (as much as possible) reproduction of the signal generated from the CD player. Thus, it is desired that the amplifier be linear one.

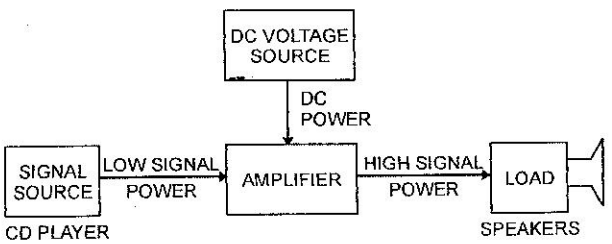


Fig. 12.1. ***Block Diagram of a Compact Disc Player System***

Figure 12.1 suggests that there are two types of analyses of the amplifier that must be considered. The first is a dc analysis because of the applied dc voltage source, and the second is a time-varying or ac analysis because of the time-varying signal source. A linear amplifier means that the superposition principle applies. The principle of superposition states : *The response of a linear circuit excited by multiple input signals is the sum of the responses of the circuit to each of the input signals alone.*

For the linear amplifier, then, the dc analysis can be performed with the ac source set to zero. This analysis.

called a *large signal* analysis, establishes the operating or Q-point of the transistors in the amplifier. This analysis and design was the primary objective of the previous chapter (Chapter 11). The ac analysis, called a *small-signal analysis,* can be performed with the dc source set to zero. The total response of the amplifier circuit is the sum of the two individual responses.

12.2. TRANSISTOR AMPLIFIER PRACTICAL CIRCUIT

A practical circuit of a single stage transistor amplifier in CE configuration and using self-biasing is shown in Fig. 12.2. The resistors R_1, R_2 and R_E form the *biasing* and stabilization circuits. The biasing circuit must establish a proper operating point otherwise a part of the –ve half cycle of the signal may be cut-off in the output. The resistor R_L connected across the output terminals is called the load. When a number of stages are employed then R_L represents the input resistance for the next stage.

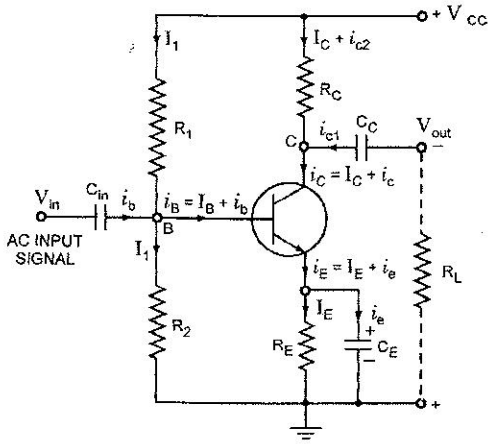


Fig. 12.2. ***Practical Circuit of a Transistor Amplifier in CE Configuration With Self-Biasing***

An electrolytic capacitor, called the *input capacitor,* C_{in} of capacity of about 10 μF is used to couple the signal to the transistor base. In the absence of this capacitor, the signal source resistance will come across R_2 and thus change the bias. This capacitor allows only ac signal to flow but isolates the signal source from R_2. Another capacitor, called the emitter bypass capacitor C_E, of capacity of about 100 μF is used in parallel with emitter resistance R_E in order to provide a low reactance path to the amplified ac signal. In the absence of this capacitor, amplified ac signal flowing through R_E will cause a voltage drop across it which in turn will feedback the input side and reduce the output voltage.

For coupling of one stage of amplifier to the next stage another capacitor C_C, called the coupling or blocking capacitor, of capacity of about 10 μF is used. Because of its presence, the output across the load resistance R_L is free from the collector dc voltage. In its absence R_C will come in parallel with the resistor R_1 of the biasing network of next stage and thereby change the biasing conditions of the next stage.

Various currents flowing in different branches of the amplifier circuit are indicated in Fig. 12.2.

With the application of input signal

Base current, i_B = DC base current due to biasing circuit + ac base current due to ac input signal

$$= I_B + i_b \quad ...(12.1)$$

Collector current, i_C = DC collector current due to biasing circuit + ac collector current due to ac input signal

$$= I_C + i_c = \beta (I_B + i_b) \quad ...(12.2)$$

Emitter current i_E = DC emitter current + ac emitter current due to ac input signal

$$= I_E + i_e \quad ...(12.3)$$

12.2.1. Emitter Bypass Capacitor. As mentioned above, it is included in the circuit to provide a low reactance path to the amplified ac signal. As shown in Fig. 12.2 it is not connected in series like a coupling capacitor, instead, it is connected across the emitter resistor R_E. The reason for doing so is to bypass or shunt ac current away from the emitter resistor R_E. When the frequency is high enough it looks like a short. Thus emitter bypass capacitor C_E is used to prevent *negative feedback* in the emitter circuit.

Very simply, negative feedback involves feeding back a portion of the amplifier *output* signal to its *input* circuit. Further, the signal is fedback in such a manner that it *opposes* the input signal. As we shall see in chapter 17, the **removal of bypass capacitor** results in an increase in the amplifier's *input resistance,* a reduction in its *voltage gain,* and an *increase* in the *output resistance* "looking into the collector". Obviously, an increase in input resistance is a step in the right direction for voltage amplifier. However, a reduction in the voltage gain and increase in the output resistance are generally undesirable effects. Yet there are some advantages offered by these sacrifices. First, even, though the voltage gain is reduced, but *stability* is increased. Specifically, it tends to be less dependent on the transistor's parameters (*e.g.*, its g_m). Second, the increase in the collector-to-ground output resistance makes our approximation of R_{out} equal to R_C even *more realistic.*

12.2.2. AC Ground. You may never have heard of an *ac ground* before, but it really does exist as a separate kind of ground that is different from a *mechanical ground.* A mechanical ground is achieved by connecting a wire between the point to be grounded and ground.

An ac ground is different because it is produced by connecting a *bypass capacitor* between the point to be shorted to ground, as far as ac signals are concerned, and the ground, this kind of ground (*i.e.* ac ground) exists only at high frequencies. In Fig. 12.2 emitter terminal is *ac grounded.* A designer uses an ac ground when any point needs to be frequency sensitive. Such a point remains normal at low frequencies but grounded at high frequencies.

12.3. PHASE REVERSAL

In a common emitter configuration, the output voltage increases in the negative direction when the input

signal increases in the positive direction and vice-versa. This is called phase reversal* and causes a phase difference of 180° between the input signal voltage V_{in} and output voltage V_{out}.

Consider a CE amplifier circuit shown in Fig. 12.3, the signal being fed at the input terminals *i.e.* between base and emitter and the output is taken from the collector and emitter ends.

The instantaneous output voltage v_{CE} is given as

$$v_{CE} = V_{CC} - i_C R_C \qquad ...(12.4)$$

Reactance of coupling capacitor C_C is negligible at ordinary signal frequencies and so it may be considered a short for the output signal.

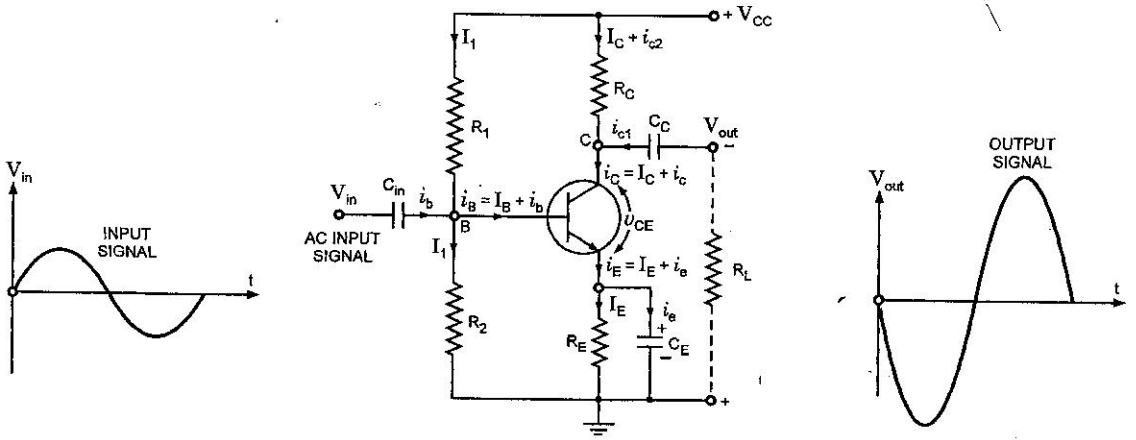


Fig. 12.3. ***Practical Circuit of a Transistor Amplifier in CE Configuration With Self-Biasing***

With the increase in the signal voltage in the positive half cycle, the base current increases causing increase in collector current and so the voltage drop $i_C R_C$. As V_{CC} is constant therefore, output voltage v_{CE} decreases. Thus we can say that as the signal voltage increases in positive direction, the output voltage increases in the negative direction *i.e.* there is a phase difference of 180° between output and input. Conversely on negative half cycle of the input signal voltage, lesser current flows through collector resistance R_C and so voltage drop across it decreases. For this reason output voltage v_{CE} increases.

The above phenomenon can be proved mathematically as below :

Differentiating Eq. (12.4), we have

$$dv_{CE} = 0 - di_C R_C$$

or $$dv_{CE} = -di_C R_C$$

The negative sign indicates that the output voltage is 180° out of phase with the input voltage.

The above fact *i.e.* phase reversal in CE configuration can be illustrated graphically with the aid of output characteristics and ac load line, as shown in Fig. 12.4. The base current varies between I_{B_1} and I_{B_2} with I_B as the zero signal base current. From figure we see that when the base current is maximum in the positive direction, v_{CE} becomes maximum in the negative direction and vice-versa. Thus, the input and output voltages are in phase opposition *i.e.* the transistor has produced a phase reversal of output voltage w.r.t. the input signal voltage.

The worthnoting points are that common base and common collector amplifiers do not produce reversal, and input and output currents are in phase in all the three configurations.

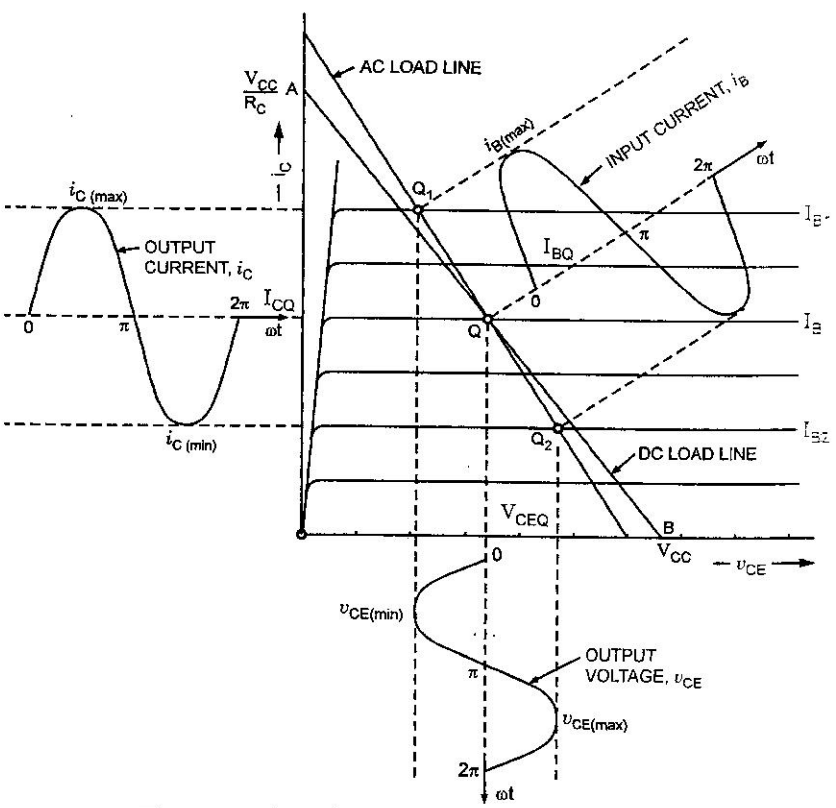


Fig. 12.4. ***Graphical Illustration of Phase Reversal***

* This will be so when output is taken from collector and emitter ends, as is always done. However if the output is taken across collector resistance R_C, it will be inphase with the input.

12.4. LOAD LINE ANALYSIS

As already discussed, the relationship between collector-emitter output voltage V_{CE} and collector current I_C is linear and, therefore, it can be represented by a straight line, on the output characteristics giving relation between V_{CE} and I_C. This is known as load line. There are two types of load lines, namely dc load line and ac load line. The former determines the values of collector current I_C and collector-emitter voltage V_{CE} corresponding to zero signal conditions whereas the latter gives their (i_C and v_{CE}) values when an ac signal is applied.

In a transistor amplifier circuit shown in Fig. 12.5, the resistors R_1 and R_2 form a voltage divider arrangement for fixing a certain dc bias voltage. This bias voltage and the emitter resistance R_E determines the emitter current I_E. The collector current I_C is almost the same as the emitter current I_E, because $I_C = I_E - I_B$ and base current I_B is negligibly small in comparison with I_C or I_E. Collector-emitter voltage V_{CE} is now determined by the collector resistance R_C.

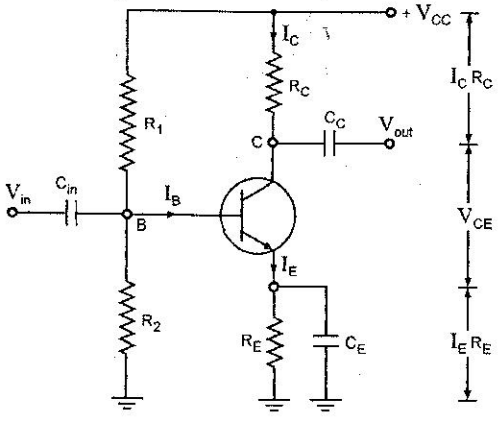


Fig. 12.5

Applying Kirchhoff's voltage law to the output section of the basic amplifier circuit shown in Fig. 12.5 we have

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$
$$= V_{CE} + I_C (R_C + R_E) \qquad \because I_C = I_E$$

$$\text{or } I_C = \frac{-V_{CE}}{R_C + R_E} + \frac{V_{CC}}{R_C + R_E} \qquad ...(12.5)$$

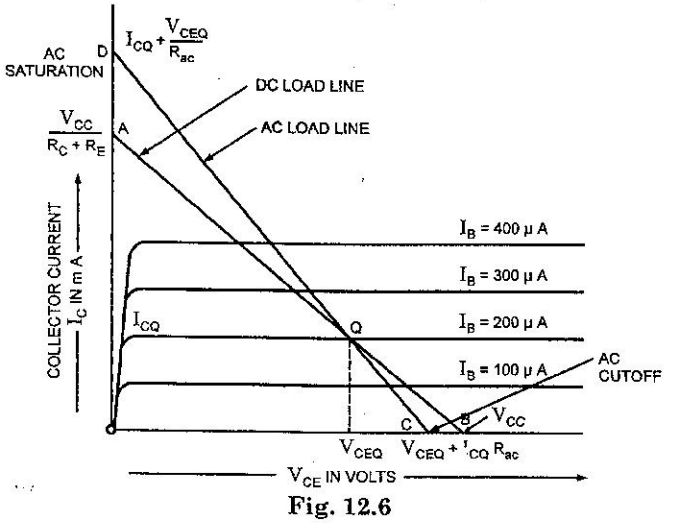


Fig. 12.6

Since V_{CC} and $(R_C + R_E)$ are constant, therefore, it represents a straight line known as dc load line. By plotting this line on the output characteristics, collector voltage V_C and collector current I_C can be determined for the given value of base current. As regards dc conditions, the amplifier circuit shown in Fig. 12.2 is reduced to that shown in Fig. 12.7. The dc equivalent circuit shown in Fig. 12.7 is so because the capacitors do not allow the flow of the direct current through them and, therefore, act as open-circuits. While drawing dc equivalent circuit it is presumed that no signal is applied.

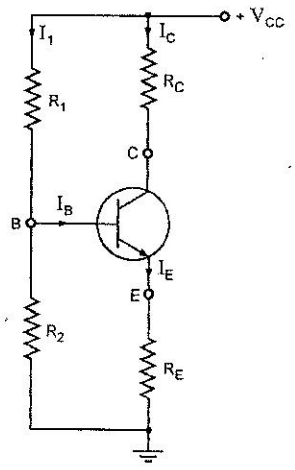


Fig. 12.7. ***DC Equivalent Circuit of Circuit Given in Fig. 12.2***

DC equivalent circuit of an amplifier circuit is drawn by reducing all the ac sources to zero and opening all the capacitors.

Any change in dc bias will change the base current which, in turn, will change the collector current I_C and collector-emitter voltage V_{CE}. As a result, the quiescent point Q shift on the dc load line. This is what roughly happens when ac signal is applied. But when ac signal is applied the variations occur very fast and the capacitors can no longer be considered as open-circuits. In fact, the variations in currents and voltages are so fast that the capacitors in the circuit may be considered as short-circuits. While dealing with ac currents and voltages (*i.e.* ac conditions), dc supplies need not to be considered. By doing so (*i.e.* reducing all the dc sources to zero and short-circuiting all capacitors), the circuit given in Fig. 12.2 is reduced to that shown in Fig. 12.8. This circuit explains the behaviour of the amplifier when viewed in ac conditions. As obvious from the figure shown in Fig. 12.8, the collector resistor R_C comes in parallel with load resistor R_L and forms the ac load for the amplifier. Now the variations in collector current and voltage are determined with the help ac load line corresponding to ac load. AC load line is different from a dc load line because ac load resistance is different from dc load resistance.

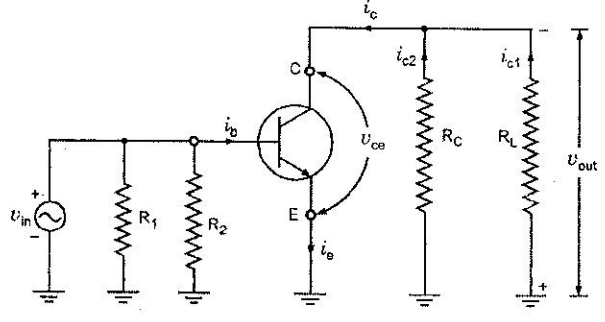


Fig. 12.8. ***AC Equivalent Circuit of Circuit Shown in Fig. 12.2***

Effective load for ac signal is given as

$$R_{ac} = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L} \quad ...(12.6)$$

When no signal is applied, the operating point is Q, as shown in Fig. 12.6. When signal is applied Q point swings along ac load line.

The saturation and cut-off points on the ac load line are different from those of dc load line. Equations for the intercepts of ac load line are derived as below.

Applying Kirchhoff's voltage law around the collector loop we have

$$v_{ce} + i_C R_{ac} = 0$$

$$\text{or } i_c = \frac{-v_{ce}}{R_{ac}} \quad ...(12.7)$$

The ac collector current is given by

$$i_c = \Delta I_C = i_C - I_{CQ}$$

and the ac collector voltage is given as

$$v_{ce} = \Delta V_{CE} = v_{CE} - V_{CEQ}$$

Substituting these equations in Eq. (12.7) we have

$$v_{CE} - V_{CEQ} + (i_C - I_{CQ}) R_{ac} = 0$$

$$\text{or } i_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} - \frac{v_{CE}}{R_{ac}} \quad ...(12.8)$$

This is the equation of the ac load line. We can find the intercepts in the usual way. When the transistor goes into saturation, v_{CE} is zero and Eq. (12.8) gives

$$i_{C\,(SAT)} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} \text{ (upper end)} \quad ...(12.9)$$

where $i_{C\,(SAT)}$ is the ac saturation current, I_{CQ} is dc collector current, V_{CEQ} is dc collector-emitter voltage and R_{ac} is the ac resistance seen by the collector.

When the transistor goes into cut-off, i_C equals zero and we get the ac cut-off voltage of

$$v_{CE\,(OFF)} = V_{CEQ} + I_{CQ} R_{ac} \text{ (lower end)} \quad ...(12.10)$$

By joining these two points line CQD can be drawn as shown in Fig. 12.6. This is the ac load line because it represents all possible ac operating points. At any instant during the ac cycle, the operating point of the transistor is somewhere along the ac load line, the exact point is determined by the amount of change that takes place from the Q point.

The slope of the ac load line is given as

$$-\frac{OD}{OC} = -\frac{I_{CQ} + \dfrac{V_{CEQ}}{R_{ac}}}{V_{CEQ} + I_{CQ} R_{ac}}$$

$$= -\frac{I_{CQ} + (V_{CEQ}/R_{ac})}{R_{ac}\left[I_{CQ} + \dfrac{V_{CEQ}}{R_{ac}}\right]} = -\frac{1}{R_{ac}} \quad ...(12.11)$$

It is seen from Fig. 12.6 that maximum possible positive signal swing is $I_{CQ} R_{ac}$ and maximum possible negative signal swing is V_{CEQ}. It means peak signal handling capacity is limited to $I_{CQ} R_{ac}$ or V_{CEQ} whichever is smaller.

Example 12.1. Draw the dc and ac load lines for the CE circuit shown in Fig. 12.9. What is the maximum peak-to-peak signal that can be obtained ?

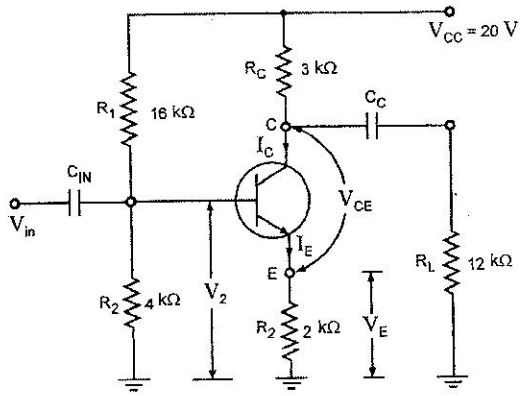


Fig. 12.9

Solution : $V_{CE\,(cutoff)} = V_{CC} = 20$ volts representing point B

$$I_C\,(\text{saturation}) = \frac{V_{CC}}{R_C + R_E} = \frac{20}{(3+2)\,k\Omega}$$

$= 4$ mA representing point A

Hence line AB gives the dc load line for the given circuit.

Approximate bias conditions can be quickly determined by assuming that base current is too small to effect the base bias.

Voltage across emitter resistance R_E,

V_E = Voltage across resistance R_2, if V_{BE} is neglected

$$\text{So } I_E R_E = V_{CC} \times \frac{R_2}{R_1 + R_2} = 20 \times \frac{4}{16+4} = 4 \text{ V}$$

$$\text{or } I_E = \frac{V_E}{R_E} = \frac{4}{2\,k\Omega} = 2 \text{ mA}$$

Collector current $I_C = I_E = 2$ mA

Hence $I_{CQ} = 2$ mA

Collector-emitter voltage,

$$V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E) = 20 - 2\text{ mA} \times (3+2)\,k\Omega = 10 \text{ V}$$

$$R_{ac} = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L} = \frac{3 \times 12}{3+12} = 2.4\,k\Omega$$

$$i_{C\,(SAT)} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}} = 2 + \frac{10}{2.4} = 6.17 \text{ mA}$$

giving saturation or upper end of ac load line

$$v_{CE\,(OFF)} = V_{CEQ} + I_{CQ} R_{ac} = 10 + 2 \text{ mA} \times 2.4\,k\Omega = 14.8 \text{ V}$$

giving cut-off point or lower end of ac load line

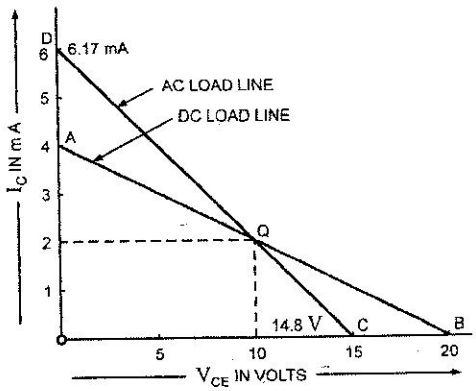


Fig. 12.10

Hence line joining 14.8 V on V_{CE} – axis and 6.17 mA on I_C – axis gives the ac load line, as illustrated in Fig. 12.10. As expected this line passes through quiescent point Q.

the physical mechanisms in the transistor and (*ii*) the values of circuit components are difficult to obtain experimentally. On the other hand, the analysis of a circuit is somewhat simpler in terms of the h-parameters than through the use of T-equivalent circuit. So T-model is not commonly used.

Example 12.6. Calculate the input and output resistances, overall current, voltage and power gains for a CE connected transistor having following *r*-parameters :
$R_s = 500\ \Omega$, $r_b = 25\ \Omega$, $r_c = 1\ M\Omega$, $r_e = 300\ \Omega$, $\alpha = 0.96$, $R_L = 10\ k\Omega$.

Solution :

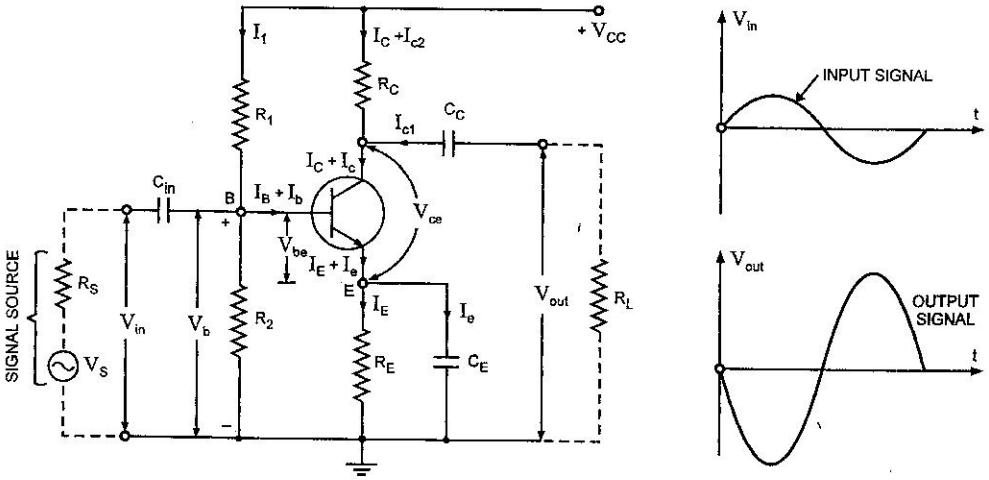


Fig. 12.30. ***Common Emitter Transistor Amplifier Circuit With Self Biasing***

$$\text{Input resistance, } R_{in} = r_b + \frac{r_e}{1-\alpha} = 25 + \frac{300}{1-0.96}$$

$$= 7{,}525\ \Omega \text{ or } 7.525\ k\Omega \textbf{ Ans.}$$

$$\text{Output resistance, } R_{out} = r_c(1-\alpha) + \frac{\alpha r_c r_e}{r_b + r_e + R_s}$$

$$= 1 \times 10^6 \times (1-0.96) + \frac{0.96 \times 10^6 \times 300}{25 + 300 + 500}$$

$$= 0.389\ M\Omega \textbf{ Ans.}$$

$$\text{Current gain, } A_i = \beta = \frac{\alpha}{1-\alpha} = \frac{0.96}{1-0.96} = 24 \textbf{ Ans.}$$

$$\text{Voltage gain, } A_v = \frac{-\alpha R_L}{r_e + (r_b + R_s)(1-\alpha)}$$

$$= \frac{-0.96 \times 10 \times 10^3}{300 + (25+500)(1-0.96)} = -30 \textbf{ Ans.}$$

$$\text{Power gain, } A_p = A_i A_v = 24 \times 30 = 720 \textbf{ Ans.}$$

12.13. ANALYSIS OF A CE TRANSISTOR AMPLIFIER USING h-PARAMETERS

Common-emitter transistor amplifier circuit with self biasing is shown in Fig. 12.30. The circuit arrangement has already been explained in Art. 12.2. Various currents flowing in different branches, and various voltages across different components and branches are indicated in the figure.

In the circuit NPN transistor is used. Input signal is applied to the base-emitter circuit while output is taken from the collector-base circuit. The emitter-base junction is forward biased and collector-base junction is reverse biased by supply V_{CC}. When the input ac signal increases in the positive direction, the voltage between base and emitter V_{be} increases because it is already positive with respect to ground. Thus forward bias is increased and causes increase in base current. Due to transistor action, collector current is increased β times. Due to flow of this current through collector resistance R_C, the voltage drop across it $I_c R_C$ increases considerably. As a result the voltage between collector and emitter V_{ce} decreases. Thus amplified voltage appears across R_L. As explained in Art. 12.3, the positive going input-signal appears as a negative going output signal *i.e.*, there is a phase shift of 180° between input and output signals. This is illustrated in Fig. 12.30.

Circuit analysis can be done rigorously using h-parameters derived from a manufacturer's data sheet for a given transistor. However, the parameters are specified only for a particular set of bias conditions and, therefore, need correction when the circuit bias conditions differ from those mentioned on the data sheet. Corrections involve use of graphs showing variation of each parameter with variations in bias conditions (I_C and V_{CE}). This process makes the analysis of even the simplest circuits quite complicated. The value of lengthy, rigorous analysis is questionable, especially when it is remembered that each h-parameter can vary significantly from one transistor to another one of the same type. For these reasons, rigorous h-parameter analysis is not taken here. Instead practical, approximate methods of determining circuit performance are treated.

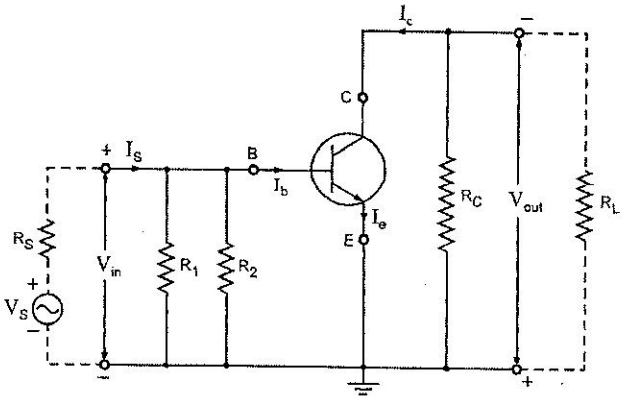


Fig. 12.31. ***CE Amplifier AC Equivalent Circuit***

AC equivalent circuit of a CE transistor amplifier shown in Fig. 12.30 is given in Fig. 12.31. From Fig. 12.31 it is obvious that the circuit input voltage V_{in} is developed across the transistor base and emitter terminals. The output is available across collector and emitter terminals. Since the emitter is common to both input and output, the circuit is designated *common emitter*, or sometimes *ground emitter circuit*.

Some CE circuit may not include bypass capacitor C_E. In such a condition unbypassed resistor R_E exists and it is to be included in the ac equivalent circuit, as shown in Fig. 12.32.

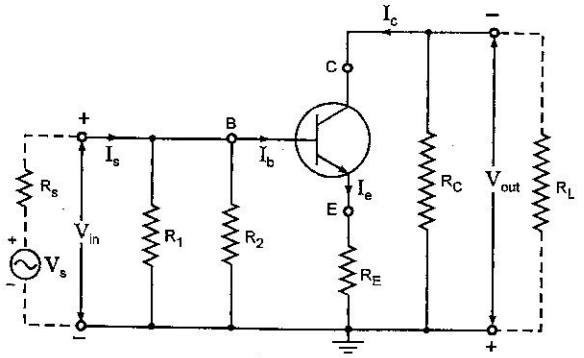


Fig. 12.32. *CE Amplifier AC Equivalent Circuit With an Unbypassed Emitter Resistor R_E*

The h-parameter equivalent of CE circuit given in Fig. 12.30 is given in Fig. 12.33. Figure 12.33 is the same as Fig. 12.31 except that the transistor has been replaced by its h-parameter equivalent circuit. When an unbypassed emitter resistor R_E is included (Fig. 12.32), the h-parameter equivalent circuit becomes as given in Fig. 12.34. Current direction and voltage polarities in Figs. 12.33 and 12.34 are those that occur when the input ac signal goes positive.

1. Input Impedance. When looking into the base emitter terminals of the transistor, h_{ie} is seen to be in series with $h_{re} V_{out}$. For a CE circuit h_{re} is normally very small quantity, so $h_{re} V_{out}$ fedback from the output to the input circuit is negligibly small as compared to the voltage drop across h_{ie}. Thus, the input impedance to the transistor base is given as

$$Z_{in\,(base)} \text{ or } Z_b = h_{ie} \qquad ...(12.43)$$

With an unbypassed emitter resistance R_E in the circuit (Fig. 12.34), the computation of Z_b becomes a little more complicated.

From circuit shown in Fig. 12.34, $h_{re} V_{out}$ being neglected, we have

$$\begin{aligned} V_{in} &= h_{ie} I_b + I_e R_E = h_{ie} I_b + R_E (I_b + I_c) \quad \because I_e = I_b + I_c \\ &= I_b h_{ie} + I_b R_E + h_{fe} I_b R_E \quad \because I_c = h_{fe} I_b \\ &= I_b [h_{ie} + R_E (1 + h_{fe})] \end{aligned}$$

and input impedance to the transistor base,

$$Z_b = \frac{V_{in}}{I_b} = h_{ie} + R_E (1 + h_{fe}) \qquad ...(12.44)$$

The actual circuit input impedance is $R_1 \parallel R_2 \parallel Z_b$, so we have

$$Z_{in} \text{ or } Z_{in\,(stage)} = R_1 \parallel R_2 \parallel Z_b \qquad ...(12.45)$$

2. Output Impedance. Since the output voltage variations have little effect upon the input of a CE circuit, only the output of the circuit need be considered in determining the output impedance. Looking back into the collector and emitter terminals of the transistor in Fig. 12.33 a large resistance $\frac{1}{h_{oe}}$ is seen. Thus, the device output impedance--

$$Z_c = \frac{1}{h_{oe}} \qquad ...(12.46)$$

The actual circuit output impedance is Z_c in parallel with R_C *i.e.*

$$Z_{out} = \frac{1}{h_{oe}} \parallel R_C \qquad ...(12.47)$$

Since $\frac{1}{h_{oe}}$ is typically 1 MΩ or so, and R_C is usually very much less than 1 MΩ, the circuit output impedance Z_{out} is approximately equal to R_C.

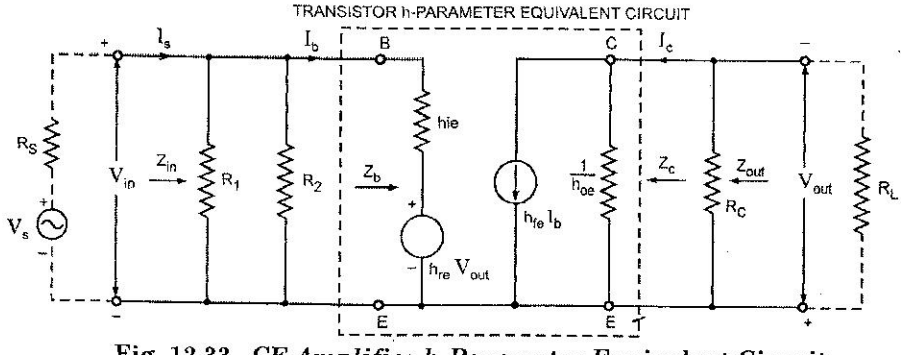


Fig. 12.33. *CE Amplifier h-Parameter Equivalent Circuit*

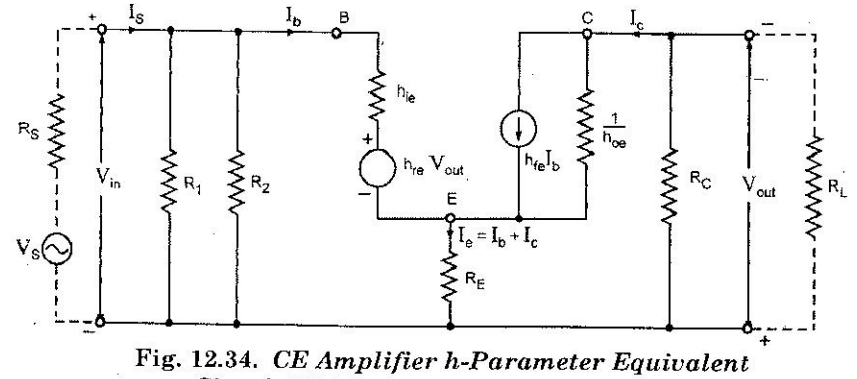


Fig. 12.34. *CE Amplifier h-Parameter Equivalent Circuit With R_E Included in The Circuit*

3. Voltage Gain. It is given as the ratio of output voltage to the input voltage

$$\text{i.e. } A_v = \frac{V_{out}}{V_{in}} = \frac{-I_c Z_{ac}}{I_b Z_{in}} = \frac{-I_c (R_C \parallel R_L)}{I_b h_{ie}}$$

$$= \frac{-h_{fe} I_b (R_C \parallel R_L)}{I_b h_{ie}}$$

$$= \frac{-h_{fe}}{h_{ie}} (R_C \parallel R_L) \qquad ...(12.48)$$

The minus sign indicates that output voltage V_{out} is 180° out of phase with input voltage V_{in}.

With an unbypassed emitter resistance R_E in the circuit (Fig. 12.34).

Ignoring $h_{re} V_{out}$ we have from the input loop of the circuit

$$\begin{aligned} V_{in} &= I_b h_{ie} + I_e R_E = I_b h_{ie} + R_E (I_b + I_c) \\ &= I_b h_{ie} + R_E I_b (1 + h_{fe}) \\ &= I_b [h_{ie} + R_E (1 + h_{fe})] \end{aligned}$$

and voltage gain,

$$A_v = \frac{-I_c (R_C \parallel R_L)}{I_b \left[h_{ie} + R_E (1 + h_{fe})\right]} = \frac{-h_{fe} (R_C \parallel R_L)}{h_{ie} + R_E (1 + h_{fe})} \quad ...(12.49)$$

Usually $R_E (1 + h_{fe}) >> h_{ie}$, therefore

$$A_v \cong \frac{-R_C \parallel R_L}{R_E} \quad ...(12.50)$$

4. Current Gain. It is given as the ratio of output current to the input current *i.e.*

$$A_i = \frac{I_L}{I_b} = \frac{-I_c}{I_b} = h_{fe} \quad ...(12.51)$$

The above equation is true for both circuits (with and without R_E). However, it is the device current gain, not the circuit current gain. From Figs. 12.33 and 12.34 it is obvious that the signal current I_S divides between R_B and Z_b where $R_B = R_1 \parallel R_2$. Using current divider equation we have

Base current, $I_b = \frac{I_s R_B}{R_B + Z_b}$ and $I_c = h_{fe} I_b = \frac{h_{fe} I_s R_B}{R_B + Z_b}$

Current gain without external load R_L in the circuit,

$$= \frac{-I_c}{I_s} = \frac{-h_{fe} R_B}{R_B + Z_b} \quad ...(12.52)$$

Overall current gain with external load R_L in the circuit,

$$A_i = \frac{I_L}{I_s} = \frac{-h_{fe} R_B R_C}{(R_C + R_L)(R_B + Z_b)} \quad ...(12.53) \because I_L = \frac{I_c R_C}{R_C + R_L}$$

5. Power Gain. $A_p = A_v A_i$ ...(12.54)

12.13.1. CE Circuit Using Fixed Bias. Common emitter transistor amplifier circuit using fixed bias is given in Fig. 12.19. The ac performance equations for the circuit given differ only slightly from those derived above. The presence of only one bias resistor makes $R_B = R_1$. This gives

$$Z_{in} = R_{in} \parallel h_{ie} \quad ...(12.55)$$

Note : For circuits using PNP transistors, the ac performance equations are exactly the same as those derived for NPN transistor circuits.

Example 12.7. A transistor amplifier is shown as under [Fig. 12.35 (*a*)]. The parameters of the transistor are $h_{ie} = 2$ kΩ, $h_{oe} = 25$ μS and $h_{fe} = 55$ and the output load resistor dissipates a signal power of 10 mW. Determine the power gain of the amplifier and the input signal emf E. The reactances of the capacitors may be neglected. Draw the equivalent circuit of the amplifier.

Solution : $Z_b = h_{ie} = 2$ kΩ

$Z_{in} = R_B \parallel h_{ie} = 80 \parallel 2 = 1.95$ kΩ

Input impedance to E, $Z_s = R_s + Z_{in} = 5 + 1.95 = 6.95$ kΩ

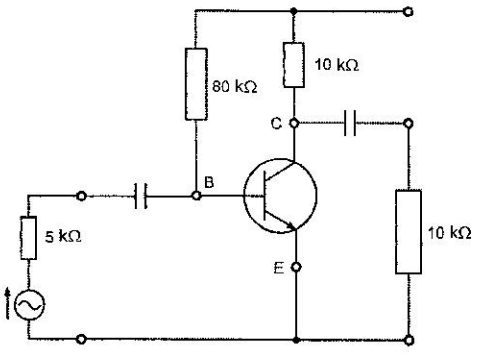
Power drawn from the source, $P_{in} = \frac{E^2}{Z_s} = \frac{E^2}{6.95}$ mW

Base current, $I_b = I_s \times \frac{R_B}{R_B + h_{ie}} = \frac{E}{6.95} \times \frac{80}{80 + 2}$

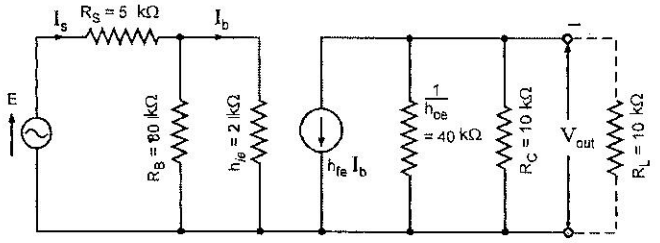
$= 0.14\,E$ (mA)

Output impedance, $Z_{out} = \frac{1}{h_{oe}} \parallel R_C = \frac{1}{25 \times 10^{-6}} \parallel 10 = 8$ kΩ

AC load resistance, $R_{ac} = Z_{out} \parallel R_L = 8 \parallel 10 = 4.44$ kΩ



(*a*)



(*b*) *AC Equivalent Circuit of Circuit Shown in Fig. 12.35 (a)*

Fig. 12.35

Output voltage, $V_{out} = -h_{fe} I_b R_{ac}$

$= -55 \times 0.14\,E \times 4.44 = -34.3\,E$ volts

Power dissipated, $P_{out} = \frac{(V_{out})^2}{R_L} = \frac{(-34.3E)^2}{10 \times 10^3}$

$= 10$ mW or 10×10^{-3} W

So $E = \frac{\sqrt{10 \times 10^{-3} \times 10 \times 10^3}}{34.3} = 0.29$ V **Ans.**

Power gain, $A_p = \frac{\text{Power dissipated}}{\text{Power input}}$

$= \frac{10 \times 10^{-3}}{\frac{E^2}{6.95} \times 10^{-3}} = \frac{10 \times 6.95}{(0.29)^2} = 826$ **Ans.**

Example 12.8. For a small signal BJT amplifier shown in Fig. 12.36, determine at 1 kHz, the following :

(*a*) quiescent collector current, I_{CQ} (*b*) small signal voltage gain, (V_0/V_i);

(*c*) maximum possible swing of the collector current. [*GATE 1999*]

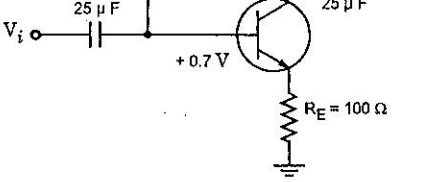


Fig. 12.36

Solution : Applying Kirchhoff's voltage law to base-emitter loop we have